

# **Universal Serial Bus 4 (USB4®) Re-Timer Specification**

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**Apple Inc.  
HP Inc.  
Intel Corporation  
Microsoft Corporation  
Renesas Corporation  
STMicroelectronics  
Texas Instruments**

**Version 2.0, Revision 1.0 RC  
November 2025**

## Release History

Version	Comments	Issue Date
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0.7	<ul style="list-style-type: none"><li>Added Re-timer Firmware Version Register in the Sideband Register space</li><li>Added clock Switch flow requirements for Gen 4</li><li>Added Recovery flow requirements for Gen 4</li><li>Added Asymmetric Transition clarifications and example</li></ul>	June 2022
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The authors of this specification would like to recognize the following people who participated in the USB4 Specification technical work group.

---

### Apple Inc. – Promoter Company Employees

Majd Abu Tayeh	Nimrod Agmon	Lior Aloni	Brian Baek
Omer Bar-Lev	Moshe Benyamini	Gopu Bhaskar	Carlos Calderon
David Conroy	Bill Cornelius	Scott Deandrea	William Ferry
Amit Flanter	Itay Franko	Radia Gantous	Alex Gerber
Mark Goikhman	Nir Guetta	Yair HersHKovitz	Scott Jackson
Husam Khashiboun	Alan Kobayashi	Alexei Kosut	Christine Krause
Dmitri Krichevsky	Alex Lozovik	Rachel Menes	Shlomi Mor
Shlomi Museri	Mona Omari	Tal Ostro	Arie Peled
Collin Pieper	Idan Reller	Reese Schreiber	Oleg Schtofenmaher
Etan Shirron	Ori Moshe Stern	Jose Tierno	Maxim Tsudik
Anatoly Uskach	Jeff Wilcox	Dan Wilson	Ohad Zalcman

---

### HP Inc. – Promoter Company Employees

Roger Benson	Marcus Benzel	Alan Berkema	Kenneth Chan
Frank Chen	Phil Chen	Hosup Chung	Glen Dower
Mark Lessman	Nam Nguyen	Roger Pearson	Kenneth Smith
Chris Tabarez			

---

### Intel Corporation – Promoter Company Employees

Nausheen Ansari	Noam Arzy	Alexandre Audier	Binata Bhattacharyya
Huimin Chen	Hengju Cheng	Salauddin Choudhury	John Crouter
Maxim Dan	Jhuda Dayan	Yoni Dishon	Eran Galil
Saranya Gopal	Venkataramani Gopalakrishnan	Raul Gutierrez	Michael Gouzenfeld
Mickey Gutman	Benjamin Hacker	Yaniv Hayat	Uri Hermoni
Alon Horn	Abdul Ismail	Abhilash K V	Ziv Kabiry
Vijaykumar Kadgi	Vijay Kasturi	Sergey Khaykin	Lev Kolomiets
Vladislav Kopzon	Efraim Kugman	Edmond Lau	Uriel Lemberger
Yun Ling	Guobin Liu	Balaji Manoharan	Liran Manor
Uma Medepalli	Assaf Mevorach	Hezi Naaman	Ohad Navon

Naod Negussie	CheeLim Nge	Leonid Plaks	Duane Quiet
Rajaram Regupathy	Reuven Rozic	Oren Salomon	Zeeshan Sarwar
Brad Saunders	Leonid Shaposhnik	Ehud Shoor	Ari Sharon
Uri Soloveychik	Einat Surijan	Aviel Uzan	Karthi Vadivelu
Alex Vekker	Chen Vrubel	Stephanie Wallick	Tzewen Wang
Sarel Wechsler	Ady Weiss	Vitaly Zhivov	Gal Yedidia
Vladimir Yudovich	Aruni P Nelson		

---

**Microsoft Corporation – Promoter Company Employees**

Randy Aull	Jim Belesiu	Martin Borve	Anthony Chen
Jesse Chen	Matt Chung	Aacer Daken	Rajib Dutta
Mark Friend	Philip Froese	David Hargrove	Robbie Harris
Kit Hui	Toby Nixon	Rahul Ramadas	Andrea Severson
Kiran Shastry	Nathan Sherman	Ji Sun	Shyamal Varma

---

**Renesas Corporation – Promoter Company Employees**

Tam Do	Robert Dunstan	Philip Leung	Kiichi Muto
Ziba Nami	Hajime Nozaki	Raman Sargis	Yoshiyuki Tomoda
Starry Tsai	Jia Wei	Toshifumi Yamaoka	

---

**STMicroelectronics – Promoter Company Employees**

Nathalie Ballot	Joel Huloux	Gerard Mas	
-----------------	-------------	------------	--

---

**Texas Instruments – Promoter Company Employees**

Mike Campbell	Anant Gole	Craig Greenburg	Michael Koltun IV
Sai Karthik Rajaraman	Anwar Sadat	Cory Stewart	Sue Vining
Deric Waters	Gregory Watkins		

---

---

**Contributor Company Employees**

---

---

<b>ACON, Advanced-Connectek, Inc.</b>	Victory Chen	Conrad Choy	Vicky Chuang
	Jessica Feng	Sharon Hsiao	Wayne Wang
<b>Advanced Micro Devices</b>	Dennis Au	Nat Barbiero	Jason Chang
	Michael Comai	Walter Fry	Will Harris
	Jason Hawken	Jim Hunkins	Ling Kong
	Scott Ogle	Victor Salim	Joseph Scanlon

	Peter Teng		
<b>Allion Labs, Inc.</b>	Howard Chang	Casper Lee	Brian Shih
<b>Analogix Semiconductor, Inc.</b>	Greg Stewart	Haijian Sui	Yueke Tang
	Ning Zhu		
<b>Anritsu Corporation</b>	Wataru Aoba	John Jerico Custodio	Kazuhiro Fujinuma
	Hiroshi Goto	Alessandro Messina	Tadanori Nishikobara
	Ryo Sunayama	Toshihiro Suzuki	Mitsuhiro Usuba
	Takeshi Wada		
<b>ASMedia Technology Inc.</b>	Chang Chinyu	Chang Weiyun	Chen Chiahsin
	Chen Chunhung	Chuang Weber	Kuo Han Sung
	Lin Curtis	Lin ShuYu	Tseng PS
	Tseng YD	Wei Daniel	Wu ShengChung
<b>Avery Design Systems, Inc.</b>	Chris Browy	Chilai Huang	Zhihong Zeng
<b>BitifEye Digital Test Solutions GmbH</b>	Sebastian Muschala	Hermann Stehling	
<b>Bizlink Technology, Inc.</b>	Alex Chou	Morphy Hsieh	Kevin Tsai
<b>Cadence Design Systems, Inc.</b>	Marcin Behrendt	Jacek Duda	Shikha Gupta
	Gaurav Jain	Poonam Khatri	Yash Kothari
	Vinod Lakshman	Shivaji Magadum	Andy Mauffet-Smith
	Rohit Mishra	Uyen Nguyen	Raja Pounraj
	Thirumal Reddy	Anand RK	Anshul Shah
	Neelabh Singh	Ofer Steinberg	Mark Summers
	Claire Ying	Wasiq Zia	
<b>Corigine, Inc.</b>	Kevin Fan	Ali Khan	Xiao Xiao
<b>Corning Optical Communications LLC</b>	Mark Bradley	Wojciech Giziewicz	Ian McKay
	Jamie Silva		
<b>Credo Semiconductor, Inc.</b>	Jim Bartenslager	Yifei Dai	Yasuo Hidaka
	Justin Lee	Phil Sun	
<b>Cypress Semiconductor</b>	Mark Fu	Naman Jain	Savan Javia
	Palani Subbiah		

<b>Dell Inc.</b>	Mohammed Hijazi	Tom Lanzoni	Ken Nicholas
	Marcin Nowak	Scott Ogle	Adie Tan
	Lee Zaretsky		
<b>Diodes Incorporated</b>	Qun Song		
<b>DisplayLink (UK) Ltd.</b>	Pete Burgers	Dan Ellis	
<b>DJI Technology Co., Ltd.</b>	Steve Huang		
<b>Electronics Testing Center, Taiwan</b>	Sophia Liu		
<b>Elka International Ltd.</b>	Alvin Cheng	Chloe Hsieh	Roy Ting
	Jui-Ming Yang		
<b>Ellisys</b>	Abel Astley	Mario Pasquali	Chuck Trefts
	Tim Wei		
<b>Etron Technology, Inc.</b>	Andy Chen	Shihmin Hsu	Bryan Huang
	Chien-Cheng Kuo	Jen Hong Larn	
<b>Foxconn / Hon Hai</b>	Patrick Casher	Joe Chen	Jason Chou
	Fred Fons	Bob Hall	Terry Little
	Christine Tran	A.J. Yang	Jie Zheng
<b>Fresco Logic Inc.</b>	Tim Barilovits	Bob McVay	Christopher Meyers
	Jie Ni	Jeffrey Yang	
<b>Genesys Logic, Inc.</b>	Sean Chen	Gerry Chou	Thomas Hsieh
	Jerry Hu	Perlman Hu	Roy Huang
	ChunYen Kuo	Weddell Lee	Jimmy Lin
	Miller Lin	D.C. Lu	Greg Tu
	Han Wu	Yihsun Wu	
<b>Google Inc.</b>	Mark Hayter	Benson Leung	Raj Mojumder
	David Schneider		
<b>Granite River Labs</b>	Nikhil Acharya	Yun Han Ang	Sandy Chang
	Allen Chen	Cyan Chen	Swee Guan Chua
	Alan Chuang	Steven Lee	Caspar Lin
	Tim Lin	Krishna Murthy	Johnson Tan

	Rajaraman V	Chin Hun Yaep	
<b>Hotron Precision Electronic Ind. Corp.</b>	Rosa Chen	Patrick Yeh	YF Zhang
<b>I-PEX (Dai-ichi Seiko)</b>	Alan Kinningham	Ro Richard	
<b>Japan Aviation Electronics Industry Ltd.</b>	Mark Saubert	Junichi Takeuchi	
<b>JMicron Technology Corp.</b>	Charon Chen	Mika Cheng	Kevin Liu
<b>Kandou Bus SA</b>	Brian Holden	Hitaish Sharma	David Stauffer
	Andrew Stewart	Mark Vennebarger	
<b>Keysight Technologies Inc.</b>	Atsushi Imaoka	Biing Lin Lem	Jit Lim
	Francis Liu	Roland Scherzinger	
<b>L&amp;T Technology Services</b>	Binu Chinna Thankam	Sunil Kumar	Siddharth Pethe
	Badrinath Ramachandra	Arunkumar Selvam	Gayathri SN
<b>LeCroy Corporation</b>	Alan Blankman	Patrick Connally	Carl Damn
	Mike Engbretson	David Fraticelli	Daniel H Jacobs
	Farnoosh Jafary	Tyler Joe	Carlo Mazzetti
	Mike Micheletti	Kathryn Morales	Jeff Sabuda
	Joseph Schachner	Chris Webb	
<b>Lenovo</b>	Toshikazu Horino	Shinji Matsushima	Yuuki Matsuura
	Nozomu Nagata	Munefumi Nakata	Kazuya Shibayama
	Shunki Sugai	Chikara Takahashi	Masahiro Tokuno
	Kayanagi Tsuneo		
<b>LG Electronics Inc.</b>	Do Kyun Kim	Yoon Jong Lee	Seung Yoo
<b>Lintes Technology Co., Ltd.</b>	Tammy Huang	Charles Kaun	RD Lintes
	Max Lo	CT Pien	Jin Yi Tu
	Jason Yang		
<b>Lotes Co., Ltd.</b>	Regina Liu-Hwang	John Lynch	
<b>Luxshare-ICT</b>	Josue Casillo	CY Hsu	Antony Lin
	John Lin	Stone Lin	Scott Shuey
	Eric Wen	Pat Young	



<b>Maxio Technology (Hangzhou) Ltd.</b>	George Fang		
<b>MediaTek Inc.</b>	Henry Chen	Alexyc Lin	Pochou Lin
	Chiachun Wang		
<b>MegaChips Corporation</b>	Rahul Agarwal	Ramesh Dandapani	Satoru Kumashiro
	Ryuichi Mariizumi	Sireesha Vemulapalli	Nobu Yanagisawa
<b>Mercedes-Benz Research &amp; Development, North America, Inc.</b>	Hans Wickler		
<b>Microchip Technology Inc.</b>	Mark Bohm	Atish Ghosh	Fernando Gonzalez
	Mark Gordon	Richard Petrie	Brigham Steele
	Anthony Tarascio	Robert Zakowicz	
<b>Molex LLC</b>	Alan MacDougall		
<b>MQP Electronics Ltd.</b>	Sten Carlsen	Pat Crowe	
<b>Newnex Technology Corp.</b>	Sam Liu		
<b>NVIDIA</b>	Jamie Aitken	Mark Overby	
<b>NXP Semiconductors</b>	Mahmoud El Sabbagh	Ken Jaramillo	Abhijeet Kulkarni
	Vijendra Kuroodi	Krishnan TN	
<b>Oculus VR LLC</b>	Marty Evans	Joaquin Fierro	Chao Hu
<b>ON Semiconductor</b>	Eduardo De Reza	Oscar Freitas	Christian Klein
	Amir Lahooti		
<b>Parade Technologies, Inc.</b>	Jian Chen	Jimmy Chiu	Mark Qu
	Craig Wiley	Paul Xu	Kevin Yuan
	Alan Yuen		
<b>Phison Electronics Corp.</b>	Jimmy Chen	Ko Hong Lipp	Sebastien Jean
	Stark Kuan	Thomas Lee	Anton Lin
	Winnie Lu	Wei Sui-Ning	James Tsai
	Michael Wu	Fu-Hua Yang	Chang Yuan-Cheng
<b>Qualcomm, Inc</b>	Tomer Ben Chen	Yiftach Benjamini	Richard Burrows
	Amit Gil	James Goel	Philip Hardy

	Raja Jagadeesan	Lalan Mishra	Dmitrii Vasilchenko
	Chris Wiesner		
<b>Realtek Semiconductor Corp.</b>	Chung-Chun Chen	Jen Wen Chen	Shen Chen
	Jonathan Chou	Chang Ding	Yao Feng
	Bokai Huang	An-Ming Lee	Ray Lee
	Ryan Lin	Terry Lin	Luobin Wang
	Kay Yin	Chris Zeng	
<b>Rohde &amp; Schwarz GmbH &amp; Co. KG</b>	Johannes Ganzert	Randy White	
<b>Samsung Electronics Co., Ltd.</b>	Jaedeok Cha	KangSeok Cho	CheolYoon Chung
	Sangju Kim	Termi Kwon	Cheolho Lee
	Edward Lee	Jun Bum Lee	Chahoon Park
	Sunggeun Yoon		
<b>Seagate Technology LLC</b>	Alvin Cox	Paul McParland	Michael Morgan
	Cuong Tran		
<b>Silicon Line GmbH</b>	Ian Jackson		
<b>SiliConch Systems Private Limited</b>	Kaustubh Kumar	Rakesh Polasa	Satish Anand Verkila
<b>Softnautics LLP</b>	Bhavesb Desai	Hetal Jariwala	Dipakkumar Modi
	Ishita Shah	Ujjwal Talati	
<b>Spectra7 Microsystems Corp.</b>	Alex Chow	James McGrath	
<b>Specwerkz</b>	Sydney Fernandes	Amanda Hosler	Diane Lenox
	Soren Petersen		
<b>STMicroelectronics</b>	Nathalie Ballot	Joel Huloux	Gerard Mas
<b>Sumitomo Electric Ind., Ltd., Optical Comm. R&amp;D Lab</b>	Sainer Siagian	Mitsuaki Tamura	
<b>Synaptics Inc.</b>	Jeff Lukanc	Mark Miller	Prashant Shamarao
<b>Synopsys, Inc.</b>	Prishkrit Abrol	Subramaniam Aravindhana	Jeanne Cai
	Jun Cao	Morten Christiansen	Scott Guo

	Eric Huang	Joseph Juan	Venkataraman Krishnan
	Jitendra Kushwaha	Behram Minwalla	Saleem Mohammad
	Rick Schmidt	Jasjeet Singh	Mahendra Singh
	John Stonick	Zongyao Wen	Fred Yu
<b>Tektronix, Inc.</b>	Madhusudan Acharya	Sourabh Das	Keyur Diwan
	Mark Guenther	Abhijeet Shinde	Gary Simontom
<b>Thine Electronics, Inc.</b>	Shuhei Yamamoto		
<b>Tyco Electronics Corp., a TE Connectivity Ltd. company</b>	Simon Li	Jeff Mason	Jacky Mo
	Tommy Yu	Yuanbo Zhang	Tony Zhu
<b>Varjo Technologies</b>	Kai Inha		
<b>VIA Labs, Inc.</b>	Wayne Tseng		
<b>VIA Technologies, Inc.</b>	Benjamin Pan	Terrance Shih	Jay Tseng
	Fong-Jim Wang		
<b>Weltrend Semiconductor</b>	Chao-Chee Ku	Jeng Cheng Liu	Wayne Lo
	Ho Wen Tsai	Eric Wu	Randolph Wu
	Simon Yeh		
<b>Western Digital</b>	David Landsman	Larry McMillan	Rob Ryan
<b>Wilder Technologies</b>	Steve Bright	Zach Moore	Joe O'Brien
	Majid Shayegh		

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## **1 Preface**

### **1.1 Scope of Document**

This specification is primarily targeted to developers of USB4® Re-timers and system OEMs. This specification can be used for developing Cable Re-timers and On-Board Re-timers.

### **1.2 Document Organization**

Chapters 1 and 2 provide an overview for all readers. Chapters 3 through 6 contain detailed technical information defining USB4 Re-timers. The following summarizes each chapter:

- Chapter 1 (Preface) – This chapter defines document conventions and terms.
- Chapter 2 (Overview) – This chapter gives an overview of the Re-timer architecture.
- Chapter 3 (Electrical Layer) – This chapter defines the requirements for electrical compliance.
- Chapter 4 (Logical Layer) – This chapter defines Lane initialization and operation.
- Chapter 5 (Port Operation) – This chapter defines the software interface to a Re-timer.
- Chapter 6 (Interoperability with Thunderbolt™ 3 Systems) – This chapter defines the requirements for a Re-timer to operate in a Link that includes Thunderbolt 3 Routers or a Thunderbolt 3 Cable.

### **1.3 Related Documents**

Universal Serial Bus (USB4®) Specification, Version 1.0 with Errata and ECN through October 15, 2020, October 2020 (USB4 Specification)

Universal Serial Bus (USB4®) Specification, Version 2.0, October 2022, (USB4 Specification v2.0)

USB Type-C® Cable and Connector Specification, Release 2.0. August 2019 (USB Type-C Specification)

Universal Serial Bus Power Delivery Specification, Release 3.0, Version 2.0, August 2019 (USB PD Specification)

### **1.4 Terms and Abbreviations**

This specification uses the same terms and abbreviations as defined in the USB4 Specification.

### **1.5 Documentation Conventions**

#### **1.5.1 Capitalization**

Some terms are capitalized to distinguish their definition in the context of this document from their common English meaning. Words not capitalized have their common English meaning.

### **1.5.2      *Italic Text***

Italic text is used to identify variable names, register field, and packet field names, or reference document titles.

### **1.5.3      Numbers and Number Bases**

Hexadecimal numbers are written with a lower case “h” suffix, e.g. FFFFh and 01h. Hexadecimal numbers larger than four digits are represented with a space dividing each group of four digits, e.g. 1EFF FFFF FFFFh. Binary numbers are written with a lower case “b” suffix, e.g. 1001b and 01b. Binary numbers larger than four digits are written with a space dividing each group of four digits, e.g. 1010 1000 1100b.

All other numbers are decimal.

### **1.5.4      Bit, Byte, DW, and Symbol Conventions**

A bit, byte, DW, or Symbol residing in location n within an array is denoted as bit[n], byte[n], DW[n], or Symbol[n].

A sequence of bits, bytes, DWs, or Symbols residing in locations n to m (inclusive) within an array is denoted as bit[m:n], byte[m:n], DW[m:n], or Symbol[m:n].

### **1.5.5      Implementation Notes**

Implementation Notes are not a normative part of this specification. They are included for clarification and illustration only. Implementation notes within this document are enclosed in a box and set apart from other text.

### **1.5.6      Word Usage**

The word “shall” is used to indicate mandatory requirements. Mandatory requirements are strictly to be followed in order to conform to this specification and no deviation is permitted.

The phrase “it is recommended” is used to convey that, among several possibilities, one is preferred but not necessarily required.

The word “may” is used to indicate a course of action permissible within the limits of the specification. The word “can” is used only for statements of possibility or capability (i.e. “can” equals “is able to”).

### **1.5.7      FourCC**

A FourCC is a sequence of four bytes used to represent ASCII strings. It is limited to ASCII printable characters (one byte per character), with space characters reserved for padding shorter sequences.

For example, the FourCC string “ABC ” is represented by a hexadecimal value of 20434241h, where the rightmost byte (41h) represents the first ASCII character (“A”).

### **1.5.8      Reserved Values and Fields**

Unless otherwise specified, fields and values marked “Rsvd” shall be handled as described in Table 1-1.



Table 1-1. Rsvd Value and Field Handling

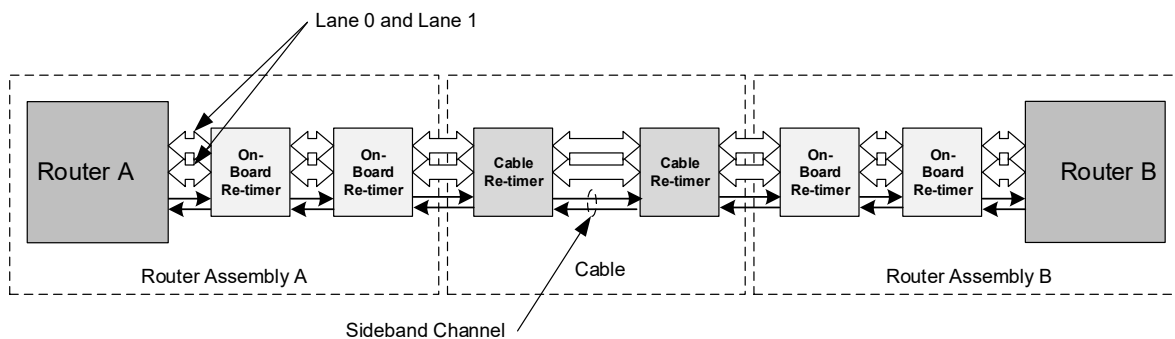
Type	Handling
Transaction Values	A transmitter shall not use a value in this specification that is marked as “Rsvd”. If a Re-timer is the only target of a Transaction, it shall ignore a Transaction that has any of its defined fields set to a Rsvd value and proceed as if the Transaction was never received.
Ordered Set Values	A transmitter shall not use a value in this specification that is marked as “Rsvd”. The target of an Ordered Set shall ignore an Ordered Set that has any of its defined fields set to a Rsvd value and proceed as if the Ordered Set was never received.

## 2 Overview

A USB4® Link supports up to six Re-timers. Of those six Re-timers, four may be On-Board Re-timers (two On-Board Re-timers at each end of the Link).

Figure 2-1 depicts a USB4 Link with six Re-timers between the two connected Routers (referred to as “Router A” and “Router B”). Router Assembly A and Router Assembly B, each include two On-Board Re-timers. The cable connecting the ends of the Link is an Active Cable with a Cable Re-timer at each end.

**Figure 2-1. USB4 Link with Re-timers**



Electrical compliance for an On-Board Re-timer is measured at the USB Type-C connector of the Router Assembly that contains the Re-timer. The electrical requirements for a Router Assembly are defined in the USB4 Specification. Additional requirements for an On-Board Re-timer are defined in Section 3.1 of this specification.

Electrical compliance for a Cable Re-timer is measured at the USB Type-C connector of the Active Cable that contains the Re-timer. The electrical requirements for an Active Cable are defined in Section 3.3 of this specification. Additional Requirements for Cable Re-timers are defined in Section 3.2 of this specification.

The Re-timer interfaces that are inside a Router Assembly or Active Cable are outside the scope of this specification.

### 2.1 External Terms and Definitions

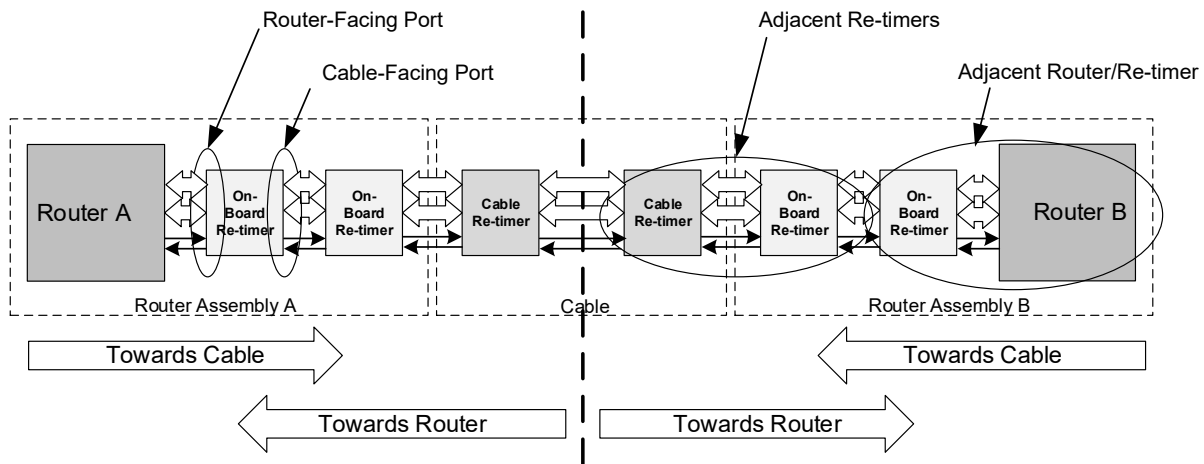
This specification uses the following terms to identify the relationships between the entities that are external to a Re-timer:

- **Router-Facing** – Describes a USB4 Port, Lane Adapter, transmitter, or receiver that faces away from the center of the Cable.
- **Cable-Facing** – Describes a USB4 Port, Lane Adapter, transmitter, or receiver that faces towards the center of the Cable.

- Adjacent – Describes a Re-timer, USB4 Port, Lane Adapter, transmitter, or receiver that is directly connected to another Re-timer, USB4 Port, Lane Adapter, transmitter, or receiver with no other Re-timers or Routers in between.

Figure 2-2 shows an example of how these terms are used.

**Figure 2-2. External Re-timer Relationships**



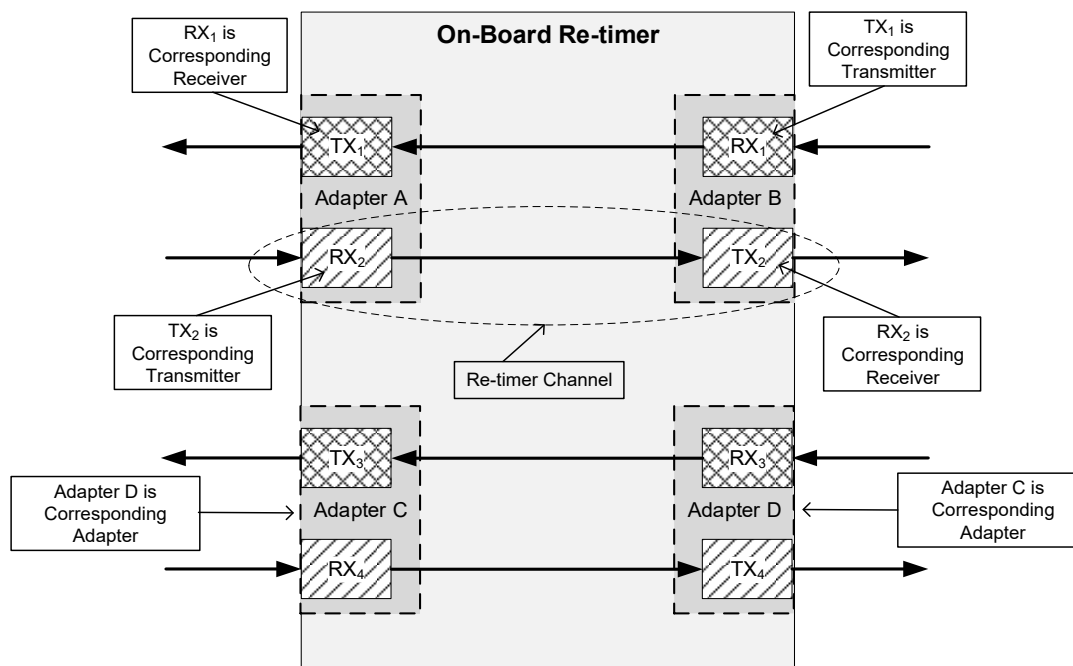
## 2.2 Internal Terms and Definitions

This specification uses the following terms to identify the relationships between the entities within a Re-timer.

- Corresponding Receiver – The receiver that feeds the transmitter with USB4 traffic.
- Corresponding Transmitter – The transmitter that accepts USB4 traffic from the receiver.
- Corresponding Adapter – The Lane Adapter that contains the Corresponding Receiver and Corresponding Transmitter.
- Re-timer Channel – a transmitter and its Corresponding Receiver, or a receiver and its Corresponding Transmitter.

Each transmitter has one Corresponding Receiver, and each receiver has one Corresponding Transmitter.

Figure 2-3. Internal Re-timer Relationships



### **3 Electrical Layer**

#### **3.1 On-Board Re-timers**

An On-Board Re-timer shall implement an Electrical Layer as defined in the USB4 Specification with the following changes:

- An On-Board Re-timer shall support Gen 2 speed of 10Gbps. Support for Gen 3 and Gen 4 speeds is optional.
- An On-Board Re-timer shall support two Lanes.
- An On-Board Re-timer operating at Gen 2 speed shall transmit a bit within  $t_{\text{Latency2}}$  after receiving the bit.
- An On-Board Re-timer operating at Gen 3 speed shall transmit a bit within  $t_{\text{Latency3}}$  after receiving the bit.
- An On-Board Re-timer operating at Gen 4 speed shall transmit a bit within  $t_{\text{Latency4}}$  after receiving the bit.
- For a pair of Corresponding Adapters, the propagation latency of one Re-timer Channel shall be within  $t_{\text{Skew}}$  of the Re-timer Channel in the opposite direction. Propagation latency is measured from the time a bit is received by a receiver until the time it is transmitted by the Corresponding Transmitter.
- An On-Board Re-timer shall add no more than  $t_{\text{Skew}}$  amount of skew on its transmitting Lanes relative to the skew measured at the receiving Lanes.

#### **3.2 Cable Re-timers**

A Cable Re-timer shall meet the requirements in the USB4 Specification with the following changes:

- A Cable Re-timer shall support Gen 2 speed of 10Gbps and Gen 3 speed of 20Gbps. Support for Gen 4 speed is optional.
- A Cable Re-timer shall support two Lanes.
- A Cable Re-timer operating at Gen 2 speed shall transmit a bit within  $t_{\text{Latency2}}$  after receiving the bit.
- A Cable Re-timer operating at Gen 3 speed shall transmit a bit within  $t_{\text{Latency3}}$  after receiving the bit.
- A Cable Re-timer operating at Gen 4 speed shall transmit a bit within  $t_{\text{Latency4}}$  after receiving the bit.
- For a pair of Corresponding Adapters, the propagation latency of one Re-timer Channel shall be within  $t_{\text{Skew}}$  of the other Re-timer Channel. Propagation latency is measured from the time a bit is received by a receiver until the time it is transmitted by the Corresponding Transmitter.

- A Cable Re-timer shall add no more than  $t_{\text{Skew}}$  amount of skew on its transmitting lanes relative to the skew measured at the receiving Lanes.
- If a Cable Re-timer supports Gen 4 speed, it shall support an Asymmetric Link as described in Section 4.4.

### 3.3 Active Electrical Cables

See the USB Type-C Specification for the electrical specifications of an Active Cable.

## 4 Logical Layer

A Re-timer shall have two USB4® Ports. USB4 Ports are defined in the USB4 Specification. The USB4 Ports on a Re-timer shall have the same number of Lane Adapters and shall support the same capabilities.



### IMPLEMENTATION NOTE

*An On-Board Re-timer needs to be aware of which USB4 Port faces towards the Router and which USB4 Port faces towards the USB Type-C connector. An On-Board Re-timer also needs to know if a USB4 Port directly interfaces a USB Type-C connector. How this knowledge is acquired is implementation specific.*

### 4.1 Sideband Channel

Sideband Channel transactions are sent and received over the SBTX and SBRX wires as defined in the USB4 Specification.

#### 4.1.1 Transactions

When forwarding Transactions from an SBRX input to an SBTX output, a Re-timer shall maintain the order of Transactions as received on the SBRX input.

##### 4.1.1.1 LT Transactions

A Re-timer shall support LT Transactions as defined in the USB4 Specification with the following changes:

- When a Re-timer receives an LT Transaction, it shall forward the Transaction to its other USB4 Port.

##### 4.1.1.2 Extended LT (ELT) Transactions

A Re-timer shall support ELT Transactions as defined in the USB4 Specification with the following changes:

- When a Re-timer receives an ELT Transaction, it shall forward the Transaction to its other USB4 Port.

##### 4.1.1.3 AT Transactions

A Re-timer shall support AT Transactions as defined in the USB4 Specification with the following changes:

- A Cable Re-timer shall forward an AT Transaction, regardless of the value of the *Recipient* bit.

- An On-Board Re-timer shall forward an AT Transaction, regardless of the value of the *Recipient* bit.
- A Re-timer shall not initiate AT Commands.

#### 4.1.1.4 RT Transactions

A Re-timer shall support RT Transactions as defined in the USB4 Specification with the changes defined in this section.

##### 4.1.1.4.1 Broadcast RT Transactions

A Router uses Broadcast RT Transactions to enumerate the Re-timers in a Link and set Re-timer Index values. The Re-timer Index is used to identify and address the Re-timers between two connected Routers. A Re-timer has two Re-timer Indexes. The Re-timer Index from a Broadcast RT Transaction received on the Router-Facing USB4 Port is referred to as the “Router-Facing Index” and the Re-timer Index from a Broadcast RT Transaction received on the Cable-Facing USB4 Port is referred to as the “Cable-Facing Index”.

*Note: The Router-Facing Index and the Cable-Facing Index for a Re-timer are not related and can have different values.*

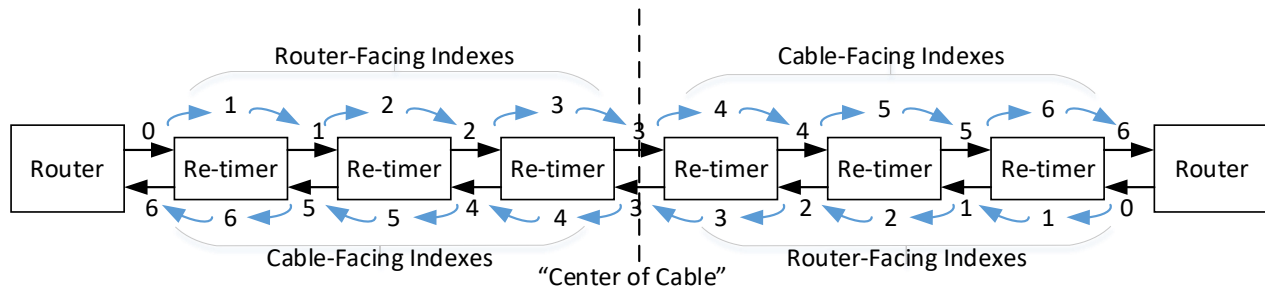
When a Re-timer receives a Broadcast RT Transaction on its Router-Facing USB4 Port, it shall increment the value in the *Index* field of the Transaction by one and shall store the resulting Re-timer Index locally as its Router-Facing Index. The Re-timer shall then forward the Broadcast RT Transaction.

When a Re-timer receives a Broadcast RT Transaction on its Cable-Facing USB4 Port, it shall increment the value in the *Index* field of the Transaction by one and shall store the resulting Re-timer Index locally as its Cable-Facing Index. The Re-timer shall then forward the Broadcast RT Transaction.

When a Re-timer forwards a Broadcast Transaction, it shall set the *SSCalways* bit to 0b to indicate that the Re-timer supports exiting CLx state with SSC turned off.

Figure 4-1 shows an example of how a Broadcast RT Transaction is used to assign Re-timer Indexes to a Link with 6 Re-timers.

**Figure 4-1. Propagation of Broadcast RT Transactions**



##### 4.1.1.4.2 Addressed RT Transactions

An On-Board Re-timer uses Addressed RT Commands to access the SB Register Space of an adjacent Router or adjacent Re-timer. When sending an Addressed RT Command, a Re-timer shall set the *Index* field to 0 to address an adjacent Router or Re-timer.

System Software also uses Addressed RT Commands to access the SB Register Space of a Re-timer.

Section 4.1.2.5 defines how Addressed RT Commands are used for Lane equalization.

The rules below define how a Re-timer handles Addressed RT Commands:

- When a Re-timer receives an Addressed RT Command with the *Index* field set to 0, it shall process the Command and send a response as described in the USB4 Specification. The Re-timer shall not forward the Transaction.
- When a Re-timer receives an Addressed RT Command on its Router-Facing USB4 Port with an *Index* field that matches its Router-Facing Index, it shall process the Command and send a response as described in the USB4 Specification. The Re-timer shall not forward the Transaction.
- When an On-Board Re-timer receives an Addressed RT Command on its Cable-Facing USB4 Port with an *Index* field that matches its Cable-Facing Index, it may process the Command and send a response as described in Section 4.1.1.24 of the USB4 Specification but is not required to do so. It shall not forward the Command.
- When a Cable Re-timer receives an Addressed RT Command on its Cable-Facing USB4 Port with an *Index* field that matches its Cable-Facing Index, it shall process the Command and send a response as described in the USB4 Specification. The Re-timer shall not forward the Transaction.
- When a Re-timer receives an Addressed RT Transaction on its Router-Facing USB4 Port with an *Index* field that does not match its Router-Facing Index, it shall forward the RT Transaction without sending a response.
- When a Re-timer receives an Addressed RT Transaction on its Cable-Facing USB4 Port with an *Index* field that does not match its Cable-Facing Index, it shall forward the RT Transaction without sending a response.
- A Re-timer shall send an RT Response within tCmdResponse time after receiving an RT Command that writes to or reads from an SB register.

The rules below define how a Re-timer handles Addressed RT Responses:

- If the *Index* field in the Addressed RT Transaction is 0, then the Re-timer shall consume the Addressed RT Response.
- If the *Index* field in the Addressed RT Transaction is not 0, the Re-timer shall forward the Addressed RT Response.

#### **4.1.1.5 SB Register Space**

A Re-timer shall maintain the SB Register Space defined in Table 4-1.



**Table 4-1. Re-timer SB Registers**

Register	Size (Bytes)	Name	Description
0	4	Vendor ID	Identifies the manufacturer of the Re-timer silicon.
1	4	Product ID	Identifies the type of the Re-timer.
2	4	Firmware Version	A vendor defined version of the Re-timer Firmware
3 to 6	N/A	Rsvd	Reserved.
7	4	LRD Tuning	Used to tune an LRD Cable.
8	4	Instruction Opcode	A Port Operation Opcode in FourCC format.
9	4	Metadata	Metadata written or read with a Port Operation.
10 to 12	N/A	Rsvd	Reserved.
13	4	Gen 2/Gen 3 TxFFE	Used to set the TxFFE parameters of transmitters for Gen 2 and Gen 3 speeds.
14	4	Gen 4 TxFFE	Used to set the TxFFE parameters of transmitters for Gen 4 speed.
15	4	Sideband Channel Version	A vendor defined version of the Sideband Channel implementation.
16 to 17	Vendor specific	Vendor specific	Vendor specific register.
18	64	Data	Data written or read with a Port Operation.
19 to 127	Vendor specific	Vendor specific	Vendor specific register.
128 to 256	N/A	Rsvd	Reserved.

Table 4-2 defines the access types for SB Register fields.

**Table 4-2. SB Register Fields Access Types**

Access Type	Description
RO	<b>Read Only.</b> An AT Write Command or an RT Write Command to a field with this access type shall have no effect. An AT Read Command or an RT Read Command shall return a meaningful value.
RW	<b>Read/Write.</b> A field with this access type shall be capable of both Read Commands and Write Commands. The value read from this field shall reflect the last value written to it unless the field was reset in the interim.
Rsvd	<b>Reserved.</b> Reserved for future implementation. A Write Command to this field shall have no effect.

The SB Register Space registers shall have the structure and fields described in Table 4-3.

**Table 4-3. SB Register Fields**

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
0	Vendor ID	0	7:0	<b>Vendor ID Low</b> Identifies the manufacturer of the Re-timer silicon.	RO	Vendor Defined
		1	7:0	<b>Vendor ID High</b> Identifies the manufacturer of the Re-timer silicon.	RO	Vendor Defined
		2	7:0	<b>Reserved</b>	Rsvd	0
		3	7:0	<b>Reserved</b>	Rsvd	0
1	Product ID	0	7:0	<b>Product ID Low</b> Assigned by the manufacturer to identify the type of the Re-timer.	RO	Vendor Defined
		1	7:0	<b>Product ID High</b> Assigned by the manufacturer to identify the type of the Re-timer.	RO	Vendor Defined
		2	7:0	<b>Reserved</b>	Rsvd	0
		3	7:0	<b>Reserved</b>	Rsvd	0
2	Version	0	7:0	<b>Version</b> Shall be set to 02h.	RO	02h
		1	7:0	<b>Minor Firmware Version</b> The binary coded decimal digit of the minor version number of the Re-timer Firmware. Contains a vendor defined value.	RO	Vendor Defined
		2	7:0	<b>Major Firmware Version</b> The binary coded decimal digit of the major version number of the Re-timer Firmware. Contains a vendor defined value.	RO	Vendor Defined
		3	7:0	<b>Reserved</b>	Rsvd	0

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
7	LRD Tuning	0	0	<b>Response Request</b> – When this bit is set to 1b by a Sideband transaction, the Port shall send a Write Command to the <i>LRD Tuning</i> register in the adjacent Router/Re-timer. The write shall contain the values of the local <i>LRD Tuning</i> and shall have the <i>Response Request</i> bit set to 0b. The USB4 Port shall then set this bit to 0b.	R/W SC	Vendor Defined
			7:1	<b>Data 0</b>	R/W	0
		1	7:0	<b>Data 1</b>	R/W	0
		2	7:0	<b>Data 2</b>	R/W	0
		3	7:0	<b>Data 3</b>	R/W	0
8	Opcode	0	7:0	<b>Opcode 0</b> Contains the first character of the Opcode.	RW	0
		1	7:0	<b>Opcode 1</b> Contains the second character of the Opcode.	RW	0
		2	7:0	<b>Opcode 2</b> Contains the third character of the Opcode.	RW	0
		3	7:0	<b>Opcode 3</b> Contains the fourth character of the Opcode.	RW	0
9	Metadata	4	7:0	<b>Metadata</b>	RW	0
13	Gen 2/Gen 3 TxFFE	0 <sup>1</sup>	3:0	<b>TxFFE Request (Lane 0)</b> Identifies one of 16 predefined TxFFE configurations requested by the receiver.	RO	Vendor Defined
			4	<b>Rx Locked (Lane 0)</b> Indicates that the receiver completed TxFFE negotiation: 0b – TxFFE negotiation is not done 1b – TxFFE negotiation is done	RO	0b

<sup>1</sup>This byte is the *Local Rx Status & TxFFE Request* byte for Lane 0

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
			5	<b>Rx Active (Lane 0)</b> Indicates whether or not the receiver is active: 0b – Receiver is inactive 1b – Receiver is active	RO	0b
			6	<b>Clock Switch Done (Lane 0)</b> Indicates whether or not the Corresponding Transmitter uses the receiver clock: 0b – Transmitter uses local clock 1b – Transmitter uses receiver clock	RO	0b
			7	<b>New Request (Lane 0)</b> Indicates whether or not the receiver is providing a new index in the <i>TxFEE Request</i> field: 0b – Receiver is still processing a previous TxFFE configuration 1b – Receiver is providing a new index in the <i>TxFEE Request</i> field	RO	0b
		1 <sup>2</sup>	3:0	<b>TxFEE Request (Lane 1)</b> Identifies one of 16 predefined TxFFE configurations requested by the receiver.	RO	Vendor Defined
			4	<b>Rx Locked (Lane 1)</b> Indicates that the receiver completed TxFFE negotiation: 0b – TxFFE negotiation is not done 1b – TxFFE negotiation is done	RO	0b
			5	<b>Rx Active (Lane 1)</b> Indicates whether or not the receiver is active: 0b – Receiver is inactive 1b – Receiver is active	RO	0b
			6	<b>Clock Switch Done (Lane 1)</b> Indicates whether or not the Corresponding Transmitter uses the receiver clock: 0b – Transmitter uses local clock 1b – Transmitter uses receiver clock	RO	0b

<sup>2</sup>This byte is the *Local Rx Status & TxFFE Request* byte for Lane 1

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
			7	<b>New Request (Lane 1)</b> Indicates whether or not the receiver is providing a new index in the <i>TxFEE Request</i> field: 0b – Receiver is still processing a previous TxFEE configuration 1b – Receiver is providing a new index in the <i>TxFEE Request</i> field	RO	0b
			2 <sup>3</sup>	<b>TxFEE Setting (Lane 0)</b> Index of the TxFEE configuration loaded the transmitter.	RO	Vendor Defined
			5:4	<b>Rsvd</b>	Rsvd	0
			6	<b>Request Done (Lane 0)</b> Indicates whether or not the transmitter loaded the recent requested index of TxFEE configuration: 0b – Transmitter has not yet loaded the recent requested index of TxFEE configuration 1b – Transmitter has loaded the recent requested index of TxFEE configuration	RO	0b
			7	<b>Tx Active (Lane 0)</b> Indicates whether or not the transmitter is transmitting a valid signal: 0b – Transmitter is not transmitting a valid signal 1b – Transmitter is transmitting a valid signal	RO	0b
			3 <sup>4</sup>	<b>TxFEE setting (Lane 1)</b> Index of the TxFEE configuration loaded the transmitter.	RO	Vendor Defined
			5:4	<b>Rsvd</b>	Rsvd	0

<sup>3</sup>This byte is the *Local Tx Status* byte for Lane 0

<sup>4</sup>This byte is the *Local Tx Status* byte for Lane 1

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
			6	<b>Request Done (Lane 1)</b> Indicates whether or not the transmitter loaded the recent requested index of TxFFE configuration:  0b – Transmitter has not yet loaded the recent requested index of TxFFE configuration  1b – Transmitter has loaded the recent requested index of TxFFE configuration	RO	0b
			7	<b>Tx Active (Lane 1)</b> Indicates whether or not the transmitter is transmitting a valid signal:  0b – Transmitter is not transmitting a valid signal  1b – Transmitter is transmitting a valid signal	RO	0b
14	Gen 4 TxFFE	See Table 4-21 in USB4 Version 2.0 Specification.				
15	Sideband Channel Version	0	7:0	<b>Sub Version</b> The binary coded decimal digit of the sub version number of the Sideband Channel implementation. Contains a vendor defined value.	RO	Vendor Defined
		1	7:0	<b>Minor Version</b> The binary coded decimal digit of the minor version number of the Sideband Channel implementation. Contains a vendor defined value.	RO	Vendor Defined
		2	7:0	<b>Major Version LSB</b> The least-significant binary coded decimal digit of the major version number of the Sideband Channel implementation. Contains a vendor defined value.	RO	Vendor Defined
		3	7:0	<b>Major Version MSB</b> The most-significant binary coded decimal digit of the major version number. Contains a vendor defined value.	RO	Vendor Defined
18	Data	64	7:0	<b>Data</b>	RW	0

#### **4.1.2 Lane Initialization**

A Re-timer shall perform Lane Initialization as described in the USB4 Specification with the modifications described in this section.

##### **4.1.2.1 Phase 1 - Determination of Initial Conditions**

During phase 1, a Re-timer discovers whether or not USB4 Mode is established on the Link.

An On-Board Re-timer shall also determine whether or not there is a reverse insertion at the Type-C connector.

A Re-timer shall not continue on to Phase 2 until it has obtained the connection information listed above. The mechanism for discovering the connection information is defined in the USB Type-C Specification and the USB PD Specification.

A Re-timer shall not proceed to phase 2 unless USB4 Mode is established on the Link.

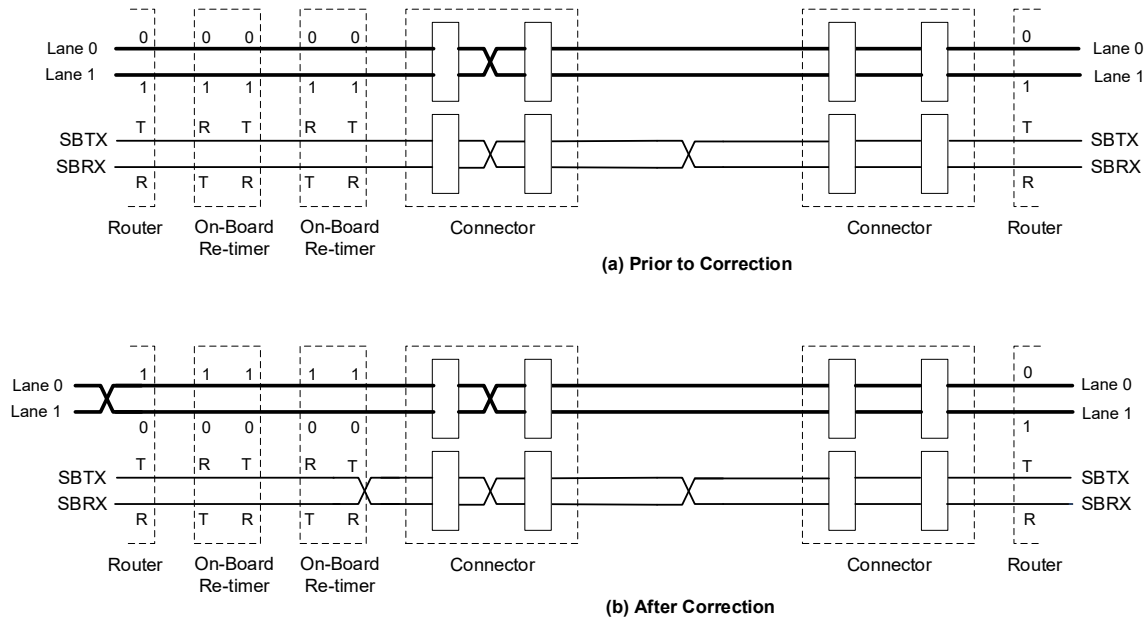
##### **4.1.2.1.1 Lane Reversal**

Lane mismatch is caused by reverse insertion of a USB Type-C connector. Lane mismatch results in Lane 0 at one end being connected to Lane 1 at the other end and the Sideband Channel SBTX (or SBRX) wires connected to each other across the Link.

When necessary to correct for Lane mismatch, Lane reversal shall take place in phase 1.

- An On-Board Re-timer that is adjacent to the USB Type-C connector shall swap its SBTX and SBRX lines facing the connector.
- An On-Board Re-timer shall swap its designation of Lane 0 and Lane 1 in both USB4 Ports.

Figure 4-2. Example of Lane Reversal



#### 4.1.2.2 Phase 2 - Router Detection

During this phase, a Re-timer determines if there is a connection on either USB4 Port.

When a Re-timer detects a logic high on SBRX of one USB4 Port for  $t_{ConnectRx}$  time, it shall drive SBTX on the other USB4 Port to logic high. The Re-timer shall then begin forwarding Transactions on the Sideband Channel in this direction.

After both USB4 Ports detect a logic high on SBRX and drive SBTX high, the Re-timer shall transition to phase 4 of Lane Initialization.

*Note: If a USB4 Port receives a Transaction while it is still in Phase 2, it may either forward and ignore the Transaction or drop the Transaction.*

#### 4.1.2.3 Phase 3 - Determination of USB4 Port Characteristics

Re-timers do not take an active role in phase 3.

#### 4.1.2.4 Phase 4 - Lane Parameters Synchronization

During phase 4, a Re-timer determines the operating characteristics of its USB4 Ports as set by the Routers. When a Re-timer receives a Broadcast RT Transaction it shall update its Link parameters to match the Link parameters in the Transaction. The Re-timer shall establish common mode voltages on its transmitters before forwarding the Broadcast RT Transaction.

*Note: The Link speed and type of Sideband Channel that an On-Board Re-timer operates with is determined only by the Broadcast Transaction it receives and is independent of the information obtained over USB PD during Phase 1 of Link Initialization.*



#### 4.1.2.4.1 Gen 2 and Gen 3

When a Re-timer detects an LT\_Resume Transaction on any USB4 Port, it shall transition to phase 5.

#### 4.1.2.4.2 Gen 4

If a Re-timer receives a Broadcast RT Transaction with the *Enable3Rx* bit set to 1b on a Port, it shall start Phase 5 as an Asymmetric Link with 3 transmitters and 1 receiver on the Port that received the Broadcast RT Transaction with the *Enable3Rx* bit set to 1b and 3 receivers and 1 transmitter on the corresponding Port. If a Re-timer receives a Broadcast RT Transaction with the *Enable3Tx* bit set to 1b on a Port, it shall start Phase 5 as an Asymmetric Link with 3 receivers and 1 transmitter in the Port that received the Broadcast RT Transaction with the *Enable3Tx* bit set to 1b and 3 transmitters and 1 receiver on the corresponding Port. If a Re-timer receives a Broadcast RT Transaction with the *Enable3Tx* bit and *Enable3Rx* bit set to 0b, it shall start Phase 5 as a Symmetric Link with 2 transmitters and 2 receivers on both Ports. The Re-timer shall set the *Start TxFFE* bit in the Tx Status byte of the Gen 4 TxFFE register in the SB Register Space of the adjacent Router/Re-timer to indicate that it is ready to start the TxFFE Receiver flow described in Section 4.1.2.5.2.

When a Re-timer Port detects LFPS on the Lane 0 receiver it shall do the following:

1. Transmit LFPS on the corresponding transmitter. A Cable Re-timer shall send the first LFPS within *tCLxForwardLFPS* time after the first LFPS cycle on the receiver. The transmitters shall send LFPS until all the following are true:
  - The Re-timer detected LFPS on Lane 0 receiver in the Port.
  - The Re-timer transmitted at least 16 LFPS cycles after detecting LFPS.
2. Transmit LFPS on the Adapter's transmitter. The first LFPS shall be sent within *tWarmUpCLx* time after the first LFPS cycle on the receiver. The transmitter shall send at least 16 LFPS cycles. The transmitter shall stop transmitting LFPS *tStopLFPS1* after detecting LFPS on its receiver.
3. After both the corresponding transmitter and the Adapter's transmitter stops sending LFPS, they shall return to Electrical Idle for *tPreData*, then all active transmitters shall start sending back-to-back Gen 4 TS1 with the *Indication* field set to 1h.
4. On each Port, after the Lane 0 receiver detects the last LFPS cycle, all enabled receivers shall be enabled for high-speed signal reception. The receivers shall be enabled *tCLxIdleRx* time after the end of the last LFPS cycle was received on Lane 0 receiver.

When all the transmitters of the Re-timer are sending Gen 4 TS1 and all the receivers of the Re-timer are enabled for high-speed signal reception, the Re-timer shall transition to Phase 5.

#### 4.1.2.5 Phase 5 - Lane Equalization

Upon entry to phase 5, a receiver shall perform the receiver flow for symmetric TxFFE negotiation as defined in the USB4 Specification. The Re-timer shall use RT Transactions (with the *Index* field set to 0b) to access the SB Register Space of the adjacent USB4 Port.

#### 4.1.2.5.1 Gen 2 and Gen 3

When the *Rx Active* bit for a receiver is set to 1b, the Re-timer shall turn on the Corresponding Transmitter and shall start transmitting CL\_WAKE1.X Symbols, where X is the Re-timer Index assigned by the Router that is the target of the CL\_WAKE1.X Symbols. The transmitter shall use a locally generated, non-SSC clock to transmit the CL\_WAKE1.X Symbols. The Corresponding Transmitter shall then perform the transmitter flow for symmetric TxFFE negotiation as defined in the USB4 Specification. The Re-timer shall use Addressed RT Transactions (with the *Index* field set to 0b) to access the SB Register Space of the adjacent USB4 Port.

The equalization flow between two Cable Re-timers is implementation specific.

#### 4.1.2.5.2 Gen 4

The enabled transmitters and receivers shall perform the transmitter and receiver flow for symmetric Gen 4 TxFFE negotiation as defined in the USB4 Specification. The Re-timer shall use Addressed RT Transactions (with the *Index* field set to 0b) to access the SB Register Space of the adjacent USB4 Port. The Re-timer's Port shall behave as follows:

1. When all the enabled receivers in the Port are ready for PAM3, all the Port's enabled transmitters shall transmit back-to-back Gen 4 TS1 with the *Indication* field set to 2h.
2. All the enabled transmitters shall transmit back-to-back Gen 4 TS2 with the *Indication* field set to 3h after all the following conditions are true:
  - Each active transmitter sends at least 16 Gen 4 TS1 with the *Indication* field set to 2h
  - All the enabled receivers detected Gen 4 TS1 with the *Indication* field set to 2h or Gen 4 TS2 or a SET\_RX\_COMPLIANCE Port Operation with *Transmitter State* field set to 010b was received.
3. When all the enabled receivers in the Port finish PAM3 TxFFE negotiation, all the enabled transmitters shall transmit Gen 4 TS2 with the *Indication* field set to 4h.

#### 4.1.2.5.3 Clock Switch

A transmitter shall start executing the Clock Switch flow as described in section 4.1.3 when all of the following are true:

- If the negotiated speed is Gen 2 or Gen 3:
  - The Re-timer has completed TxFFE negotiation for all transmitters in that USB4 Port and all their Corresponding Receivers.
  - The *Clock Switch Done* bit for Lane 0 of the adjacent USB4 Port is 1b.
- If the negotiated speed is Gen 4, tTS3Detect time after all the following conditions are true:

- All the enabled receivers in the corresponding Port detected Gen 4 TS3 or a SET\_RX\_COMPLIANCE Port Operation with *Transmitter State* field set to 011b was received.
- All enabled receivers in the corresponding Port that detected Gen 4 TS3 or SET\_RX\_COMPLIANCE Port Operation with *Transmitter State* field set to 011b and their corresponding transmitters have completed TxFFE negotiation.
- All receivers in the Port detected Gen 4 TS2 with *Indication* field set to 4h or Gen 4 TS3 or SET\_TX\_COMPLIANCE Port Operation with *Forward* bit set to 1b.

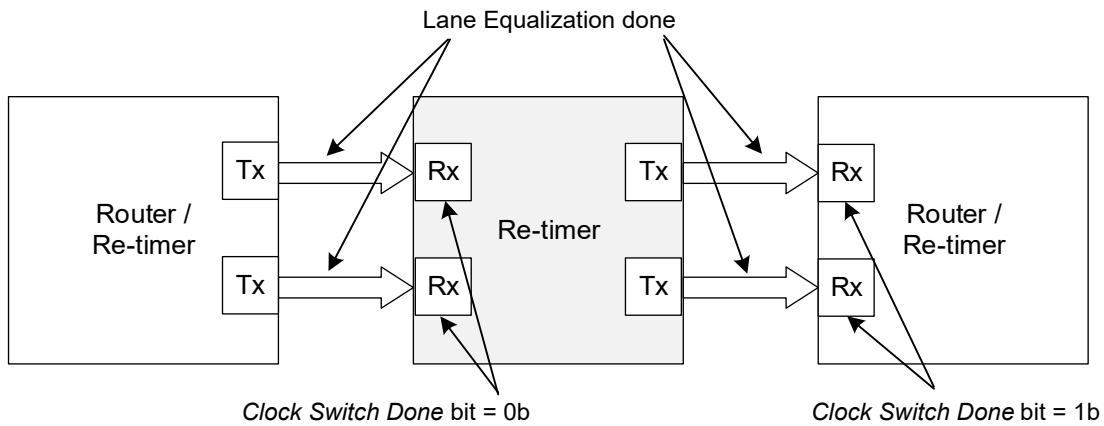
#### 4.1.3 Clock Switch Flow

##### 4.1.3.1 Gen 2 and Gen 3 Clock Switch Flow

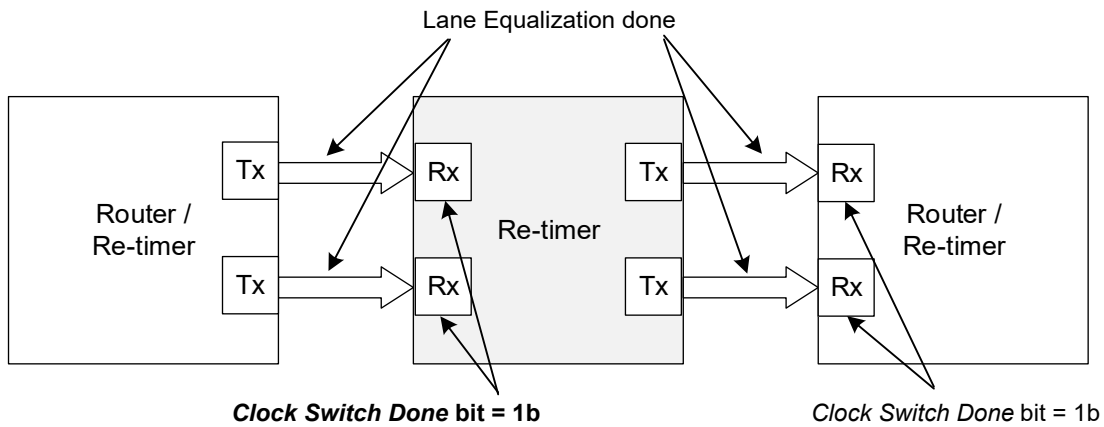
The transmitters shall stop using the local clock and shall start using the recovered clock from the Corresponding Receiver. The transition may or may not take place on Symbol boundary.

After a transmitter switches to using the receiver clock, it shall forward the bit stream it receives from the Corresponding Receiver instead of transmitting its locally-generated patterns. If there is more than one Re-timer on the Link, the Channel's receiver may lose alignment during the Clock Switch flow of other Re-timer(s)/ The Re-timer shall complete Symbol Realignment of the SLOS Ordered Sets within tSymbolLockRT time. The Re-timer shall set the *Clock Switch Done* bit in the Corresponding Receiver to 1b. Figure 4-3 shows how the *Clock Switch Done* bits are set.

Figure 4-3. Progression of Clock Switch Done Bit



(a) Before clock switch in Re-timer



(b) After clock switch in Re-timer

During the transition from local clock to receiver clock, the Re-timer shall meet the frequency variation requirements as specified in the USB4 Specification (see Section 3.1.3.1.1). The transition may or may not take place on a Symbol boundary.

#### 4.1.3.2 Gen 4 Clock Switch Flow

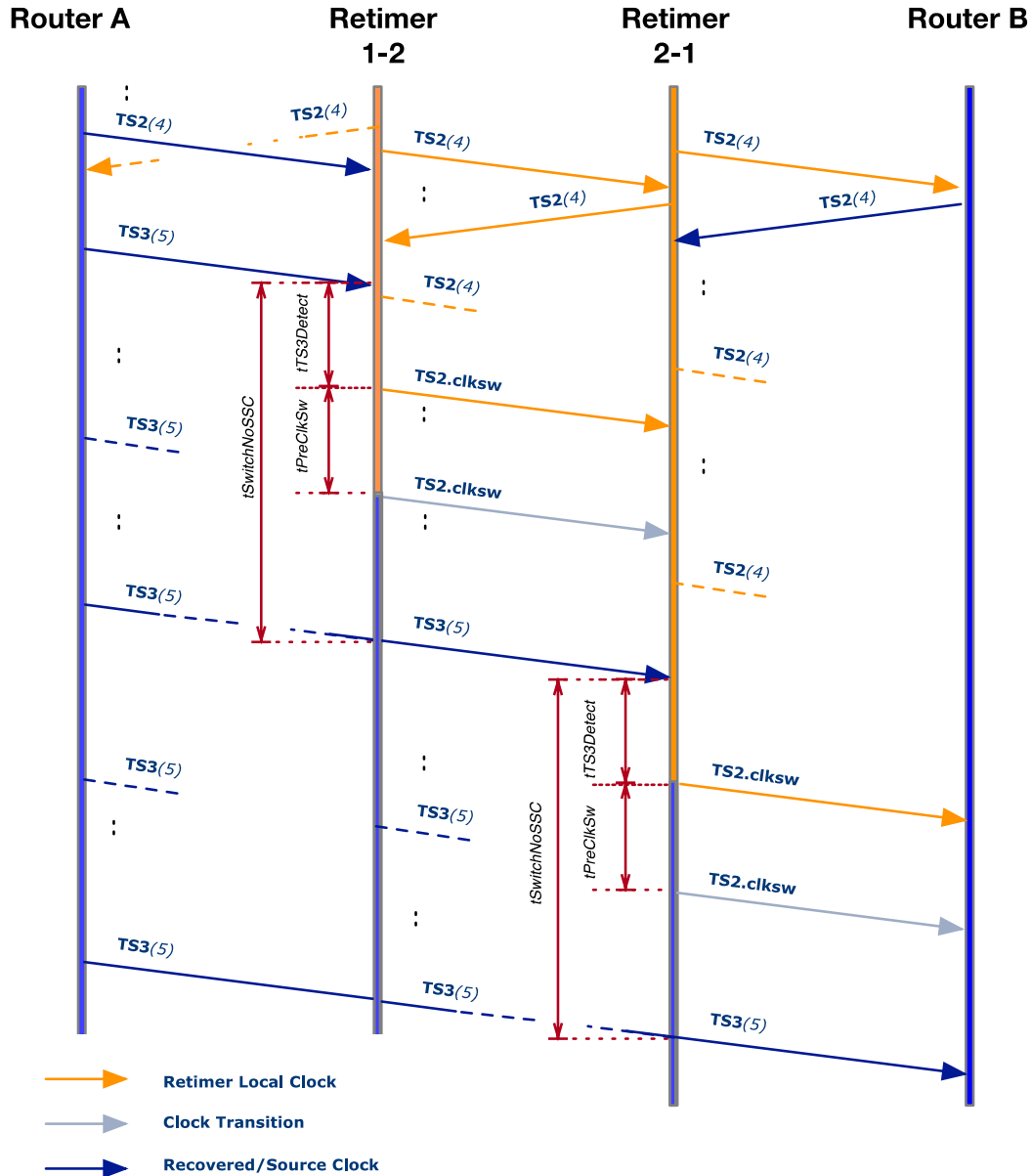
Clock Switch Flow applies to a Re-Timer channel, once the following conditions are satisfied:

- Lane Initialization, as defined in 4.1.2.5.3
- Low Power state exit, as defined in 4.2.4.3.2

The channel's active transmitters transition from sending Gen 4 TS2 with *Indication* field set to 4h to sending back-to-back Gen 4 TS2.clksw using the local clock. Gen 4 TS2.clksw is defined in the USB4 Specification (see Section 4.2.1.3.5.3). The transition from Gen 4 TS2 to Gen 4 TS2.clksw may or may not take place on Symbol boundary. After sending Gen 4 TS2.clksw with local clock for tPreClkSw time, the transmitters shall transition to using the recovered clock from the Corresponding Receivers while continuing to send Gen 4 TS2.clksw. During the transition from local clock to receiver clock, the Re-timer shall meet the frequency variation requirements as specified in the USB4 Specification (see Section 3.2.3.10). The transition from local to recovered clock may or may not take place on a Symbol boundary. The transmitters shall complete the switch from the local clock to the recovered clock within tSwitchNoSSC from receiving the Gen 4 TS3. The transmitters shall switch to forwarding the received trit stream from the Corresponding Receiver instead of transmitting its locally generated patterns after completion of the clock switch. When forwarding the trit stream from the Corresponding receiver, the transmitters shall meet the clock requirements as specified in the USB4 Specification (see Table 3-22 in Section 3.2.3).

Figure 4-4 shows an example on a Gen 4 Clock Switch from Router A to Router B on an exit from CL1.

Figure 4-4. Gen 4 Clock Switch Example



## 4.2 Re-timer Channel State Machine

This section defines the state machine of a Re-timer Channel. Unlike the USB4 Specification, this specification describes the progression of a Re-timer Channel rather than of a Lane Adapter. For a Gen 4 Link, the Re-timer Channel State Machine on both Channels shall be synchronized to the same state.

A Re-timer Channel shall support the following states:

- CLd state - The Re-timer Channel starts Lane Initialization as defined in Section 4.1.2
- Bit Lock state - The Re-timer Channel is performing bit synchronization
- Forwarding state - The Re-timer Channel forwards traffic from its receiver to its transmitter
- CL0s, CL1, CL2 states - The Re-timer Channel is in a low power state

The state machine in Figure 4-5 describes the behavior of a Re-timer Channel for Gen 2 and Gen 3 Links. The state machine in Figure 4-6 describes the behavior of a Re-timer Channel for Gen 4 Links. A detailed description of the states and transitions between states follows.

**Figure 4-5. The Re-timer Channel State Machine (Gen 2 and Gen 3)**

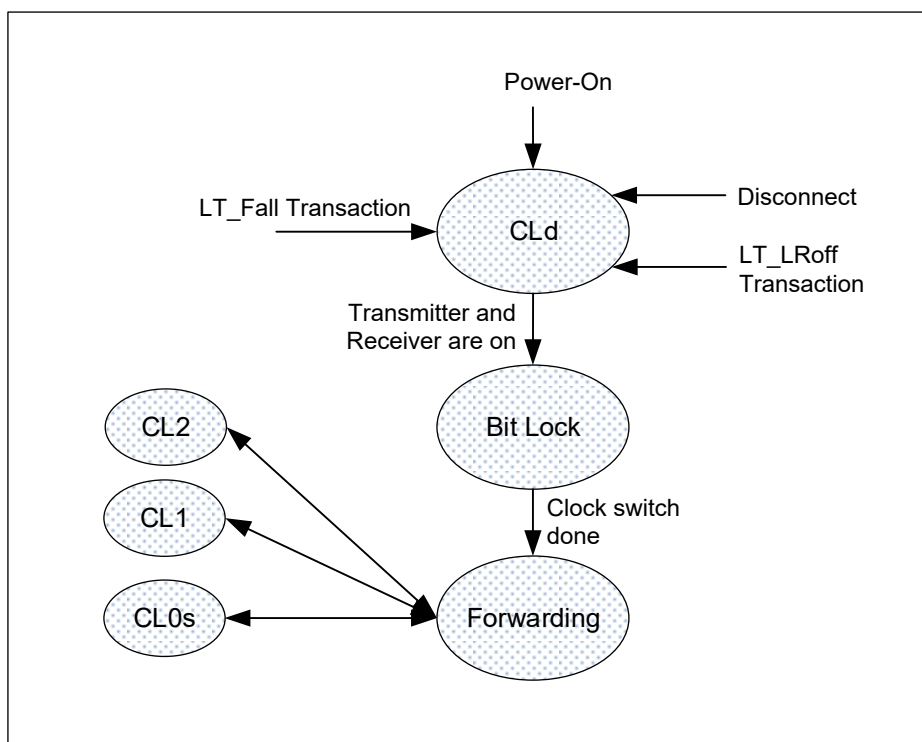
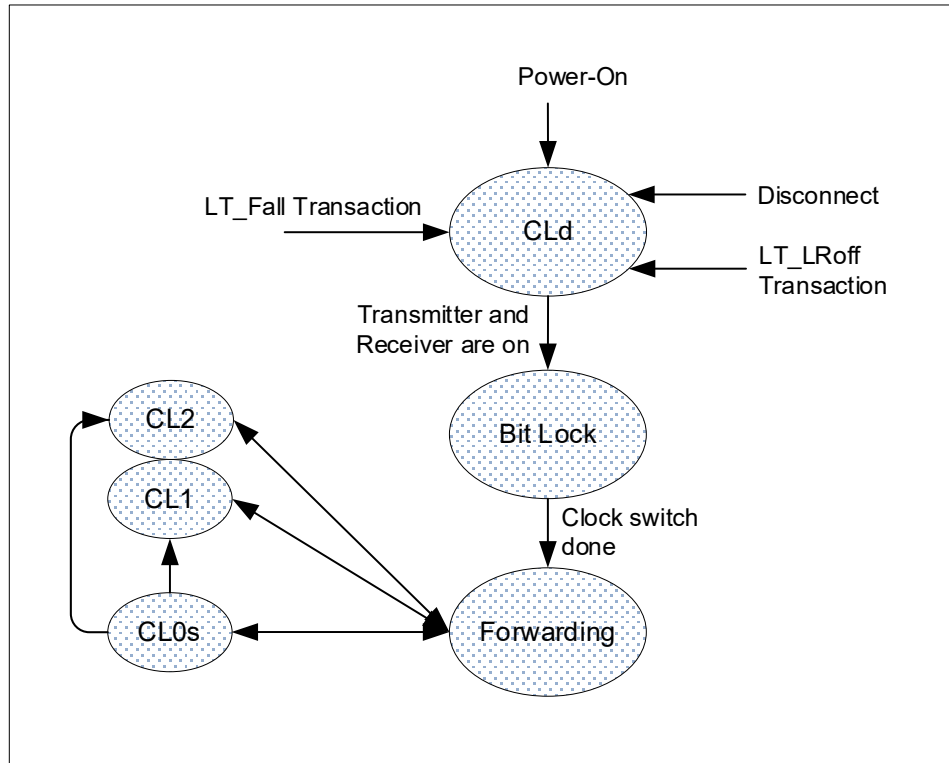


Figure 4-6. The Re-timer Channel State Machine (Gen 4)



#### 4.2.1 CLd

##### 4.2.1.1 Entry to State

A Re-timer Channel shall transition to the CLd state when any of the following occur:

- The Re-timer is first powered on.
- The Re-timer detects a disconnect event (i.e. SBRX transitions to logical low on any USB4 Port for more than  $t_{DisconnectRx}$  time).
- The SBRX of both Re-timer USB4 Ports are at logical high and both USB4 Ports receive an LT\_LRoff Transaction within  $t_{LRoff}$  of each other.
  - This is the case where a Domain enters Sleep state with wake enabled on the Link. The Re-timer shall store the last set of TxFFE parameters used prior to entry to CLd state in order to shorten exit time from this state.
- The Re-timer Channels for Lane 0 shall also transition to CLd state when the Re-timer receives an LT\_Fall Transaction on any USB4 Port with *LSELane* field set to 0b.
- The Re-timer Channels for Lane 1 shall also transition to CLd state when the Re-timer receives an LT\_Fall Transaction on any USB4 Port with *LSELane* field set to 1b.



- Received an ELT\_Recovery Transaction.

*Note: The LT\_Fall Transaction is not relevant when Link is in Gen 4.*

A Re-timer Channel that transitions to CLd state due to an LT\_Fall Transaction shall maintain any Lane state acquired in phase 1 and phase 2 of the previous Lane Initialization.

A Re-timer Channel that transitions to CLd state due to an ELT\_Recovery Transaction shall maintain any Lane state acquired in phases 1 to 5 of the previous Lane Initialization, including TxFFE Presets used by the transmitters.

#### **4.2.1.2 Behavior in State**

A Re-timer Channel does not need to maintain Lane common mode voltages while in CLd state.

When Lane Initialization begins:

- If the Re-timer Channel entered this state after power-on, then Lane Initialization starts unconditionally and in phase 1.
- If the Re-timer Channel entered this state after detecting a disconnect event, or if a disconnect event occurred while in CLd state, then a connect event starts Lane Initialization in phase 1.
- If the Re-timer Channel entered this state after detecting LT\_LRoff Transactions, then detection of a Broadcast RT Transaction by any USB4 Port starts Lane Initialization in phase 4.
  - During Lane Initialization, the Re-timer shall start phase 5 with the last set of TxFFE parameters used prior to entry to CLd state.

#### **4.2.1.3 Exit from State**

A Re-timer Channel shall exit this state when its transmitter is transmitting and its receiver is enabled.

After exiting the CLd state, a Re-timer Channel shall transition to the Bit Lock state.

### **4.2.2 Bit Lock**

#### **4.2.2.1 Entry to State**

A Re-timer Channel shall enter this state upon any of the following event:

- After exiting the CLd state.

#### **4.2.2.2 Behavior in State**

A Re-timer Channel's receiver achieves bit synchronization, receiver equalization, and clock switch to the recovered clock during this state.

The transmitter and receiver are on while in this state.

#### **4.2.2.3 Exit from State**

A Re-timer Channel shall exit this state after its receiver achieves bit lock and its transmitter is transmitting the bit stream received by its receiver.

After exiting the Bit Lock state, a Re-timer Channel shall transition to the Forwarding state.

### **4.2.3 Forwarding**

#### **4.2.3.1 Entry to State**

A Re-timer Channel shall enter this state upon any of the following events:

- Successful completion of receiver lock in CLd state.
- Exit from CLx state.

#### **4.2.3.2 Behavior in State**

When a Re-timer Channel is in Forwarding state, it shall forward traffic from its receiver to its corresponding transmitter. A Re-timer shall forward traffic regardless of whether or not it receives Logical Layer Symbols. For example, during compliance testing, a Re-timer forwards PRBS31 pattern instead of Logical Layer Symbols.

*Note: A Re-timer does not support entry to Low Power states when it is forwarding traffic that is not Logical Layer Symbols.*

A Re-timer Channel shall not modify the logical level of a bit or trit. A Re-timer Channel shall neither add nor discard any bits or trits.

#### **4.2.3.3 Exit from State**

A Re-timer Channel shall exit this state after one of the following occurs:

- Transition to the CLd state (see Section 4.2.1.1).
- Transition to the CL0s, CL1, or CL2 states.

### **4.2.4 Low Power (CL0s, CL1, and CL2)**

The CL0s, CL1, and CL2 Low Power states are used to reduce transmitter and receiver power when a Lane is idle. A Cable Re-timer shall support the CLx Low Power states. An On-board Re-timer may optionally support the CLx Low Power states.

When a Router Lane Adapter transitions to CL0s state, any Re-timer Lane Adapters on the Link transition one Re-timer Channel to CL0s state and leave the other Re-timer Channel in CL0.

When a Router Lane Adapter enters CL1 state, any Re-timer Lane Adapters on the Link transition both their Re-timer Channels to CL1 state.

When a Router Lane Adapter enters CL2 state, any Re-timer Lane Adapters on the Link transition both their Re-timer Channels to CL2 state.

#### **4.2.4.1 Entry to State**

A Lane Adapter follows the rules in this section to transition its Re-timer Channels to CL2, CL1, or CL0s state. See the USB4 Specification for the definitions of the Ordered Sets used in this section. See Appendix A for several examples of Re-timer behavior during entry to low power state.

##### **4.2.4.1.1 Gen 2 and Gen 3 Entry to Low Power State**

Rules for low power state entry:

- On detection of 3 back-to-back CL2\_ACK Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units. This counter is called the “CL2\_ACK Counter”. The initial value of CL2\_ACK Counter shall be the number of CL2\_ACK Ordered Set Symbols that were already forwarded.
- On detection of 3 back-to-back CL1\_ACK Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units. This counter is called the “CL1\_ACK Counter”. The initial value of CL1\_ACK Counter shall be the number of CL1\_ACK Ordered Set Symbols that were already forwarded.
- When the CL2\_ACK Counter reaches a count of  $t_{RxShut}$  it may shut down the Channel’s receiver. While the receiver is shut down and the Channel still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use a local clock without SSC. When the CL2\_ACK Counter reaches a count of  $t_{EnterCLx}$ , the Re-timer Lane Adapter shall:
  - Transition the Re-timer Channel in the direction forwarding the CL2\_ACK Ordered Sets to a CL2 state.
  - Reset the CL2\_ACK Counter.
  - Transition the Re-timer Channel transmitter to electrical idle within  $t_{RtTxOff}$  time from expiration of the CL2\_ACK Counter.
  - Wait  $t_{EnterLFPS1}$ , then enable detection of Low Frequency Periodic Signaling (LFPS).
- When the CL1\_ACK Counter reaches a count of  $t_{RxShut}$  it may shut down the Channel’s receiver. While the receiver is shut down and the Channel still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use local clock without SSC. When the CL1\_ACK Counter reaches a count of  $t_{EnterCLx}$ , the Re-timer Lane Adapter shall:
  - Transition the Re-timer Channel in the direction forwarding the CL1\_ACK Ordered Sets to a CL1 state.
  - Reset the CL1\_ACK Counter.
  - Transition the Re-timer Channel transmitter to electrical idle within  $t_{RtTxOff}$  time from expiration of the CL1\_ACK Counter.

- Wait  $t_{\text{EnterLFPS1}}$ , then enable detection of Low Frequency Periodic Signaling (LFPS).
- On detection of 3 back-to-back CL\_OFF Ordered Sets, the Re-timer Lane Adapter shall start counting time in Symbol Time units. This counter is called the “CL\_OFF Counter”. The initial value of CL\_OFF Counter shall be the number of CL\_OFF Ordered Set Symbols that were already forwarded.
- When the CL\_OFF Counter reaches a count of  $t_{\text{RxShut}}$  it may shut down the Re-timer Channel’s receiver. While the receiver is shut down and the Re-timer Channel is still in Forwarding state, the transmitter shall transmit a DC balanced signal and may use local clock without SSC. When the CL\_OFF Counter reaches a count of  $t_{\text{EnterCLx}}$ , the Re-timer Lane Adapter shall:
  - Transition the Re-timer Channel in the direction forwarding the CL\_OFF Ordered Sets to a low power state as follows:
    - If CL2\_ACK Ordered Sets were detected during the entry flow, transition to CL2 state.
    - If CL1\_ACK Ordered Sets were detected during the entry flow, transition to CL1 state.
    - If CL0s\_ACK Ordered Sets were detected during the entry flow, transition to CL0s state.
  - Reset the CL\_OFF Counter.
  - Transition the Re-timer Channel transmitter to electrical idle within  $t_{\text{RtTxOff}}$  time from expiration of the CL\_OFF Counter.
  - Wait  $t_{\text{EnterLFPS1}}$ , then enable detection of Low Frequency Periodic Signaling (LFPS).

A Re-timer Lane Adapter shall respond to Logical Layer Errors as defined in Section 4.3.1.

*Note: The detection latency might be greater than the forwarding latency, hence the initial value of the Counters may be greater than 3.*

If a Re-timer Lane Adapter detects 15 back-to-back SLOS Symbols, it shall abort the entry flow. The Re-timer Lane Adapter shall also reset the CL2\_ACK Counter and the CL1\_ACK Counter to zero.

*Note: Error scenarios during the CLx entry flow are handled by the Routers and may cause Link disconnect.*



#### IMPLEMENTATION NOTE

*When the transmitter at the other end of a Lane stops forwarding after  $t_{\text{RxShut}}$  or is transitioning to electrical idle during entry to CL2, CL1, or CL0s states, the received signal may be invalid. It is recommended that a Re-timer not update its PHY parameters during that time to avoid capturing stale values.*

#### 4.2.4.1.2 Gen 4 Entry to Low Power State

The Channel's transition to the CL1 and CL2 states is always after the Channel on the other direction is already in CL0s state. When entry to the CL0s state occurs with Gen 4 CL\_OFF and with the *CL State* field set to 2t, it is referred to as "CL0s with option to CL2". Otherwise, it is referred to as "CL0s with option to CL1".

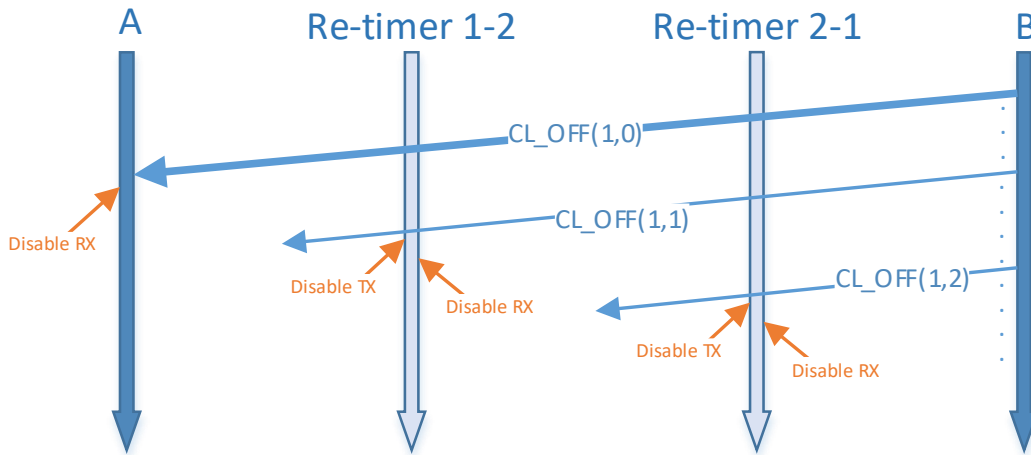
Rules for low power state entry:

- On detection of a Gen 4 CL\_OFF Ordered Set on the Lane 0 receiver with an *Index* field that matches the Index given to the Re-timer by the Router to which the Re-timer forwards the Gen 4 CL\_OFF Ordered Set, the Re-timer shall:
  1. Shut down all enabled transmitters that forwarded the Gen 4 CL\_OFF within  $t_{RtTxOff}$  time after forwarding the first trit of the first Gen 4 CL\_OFF Ordered Set on Lane 0. Not enable LFPS transmission before  $t_{EnterLFPS1}$  time has elapsed after shutting down all enabled transmitters.

*Note: On Lane 0, the previous Gen 4 CL\_OFF Ordered Set is forwarded completely. Due to Lane-to-Lane skew, it is possible that the Tx1 and/or Tx2 (if enabled) will not finish the 126 CL\_OFF Ordered Sets before shutting down.*
  2. Disable LFPS detection on the Lane 0 receiver when Gen 4 CL\_OFF is detected. Shut down all enabled receivers before receiving the last trit of last CL\_OFF Ordered Set on Lane 0 receiver. Enable LFPS detection on the Lane 0 Receiver  $t_{EnterLFPS2}$  time after Gen 4 CL\_OFF is detected.
  3. Both directions in the Re-timer shall enter the CL2 state if all the following are true:
    - The opposite direction is in CL0s with option to CL2.
    - The *CL State* field in the detected Gen 4 CL\_OFF is set to 2t.
  4. Else, both directions of the Re-timer shall enter the CL1 state if the opposite direction is in CL0s.
  5. Else, the Re-timer shall enter the CL0s state and retain the *CL State* field in the detected Gen 4 CL\_OFF Ordered Set.

Figure 4-7 shows an example of a CL0s entry flow. In this example there are 2 Re-timers on the Link between Router A and Router B. Re-timer 1-2 is assigned Index 1 from Router A and Index 2 from Router B. When a Re-timer detects a Gen 4 CL\_OFF with the *Index* field set to 1t that matches the Index given to it by Router A, it shuts down its transmitter and receiver.

Figure 4-7. Low Power State Entry Example



#### IMPLEMENTATION NOTE

*When the transmitter at the other end of a Link stops forwarding after  $t_{RxShut}$  or is transitioning to electrical idle during entry to the CL2, CL1, or CL0s states, the received signal may be invalid. It is recommended that a Re-timer not update its PHY parameters during that time to avoid capturing stale values.*

#### 4.2.4.2 Behavior in State

While a Re-timer Channel is in CL2 state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.

While a Re-timer Channel is in CL1 state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.

While a Re-timer Channel is in CL0s state, its transmitter shall be in electrical idle. Lane common mode voltages shall be maintained.

#### 4.2.4.3 Exit from State

A Re-timer follows the rules in this section when a Re-timer Channel exits from CL2, CL1, or CL0s state. See the USB4 Specification for examples of end-to-end flows describing the behavior of Re-timers during CL2, CL1, or CL0s exit.

The exit flows from the CL0s, CL1, and CL2 states for Gen 2 and Gen 3 Links are described in Section 4.2.4.3.1. The exit flows from the CL0s, CL1, and CL2 states for Gen 4 Links are described in Section 4.2.4.3.2.

##### 4.2.4.3.1 Gen 2 and Gen 3 Exit from State

###### 4.2.4.3.1.1 CL0s Exit

This section describes Re-timer behavior during CL0s exit for a Gen 2 or Gen 3 Link.

When a Re-timer detects an LFPS burst on one of its receivers, the Re-timer shall:

1. Send a Low Frequency Periodic Signaling (LFPS) burst from the Corresponding Transmitter. The duration of the LFPS burst shall be at least 16 LFPS cycles and no more than  $t_{LFPSDuration}$ . A Cable Re-timer shall transmit the first LFPS  $t_{CL1ForwardLFPS}$  time after the first cycle of LFPS on the receiver.
2. Return the Corresponding Transmitter to Electrical Idle for  $t_{PreData}$ .
3. Enable the receiver to start calibration. The Re-timer shall not enable the receiver until at least  $t_{CLxIdleRx}$  after the last LFPS cycle was received.
4. Start sending  $CL\_WAKE1.X$  Symbols from the Corresponding Transmitter, where X is the Re-timer Index assigned by the Router that is the target of the  $CL\_WAKE1.X$  Symbols. The Re-timer shall transmit the Symbols using a locally generated, non-SSC, clock.

After a Re-timer receives 3 back-to-back  $CL\_WAKE2.X$  Symbols (where X is the same value as in step 4) on at least one Lane Adapter, the Re-timer shall transition each Re-timer Channel that is in  $CL0s$  state to transmit on the clock recovered from the received Symbols rather than on its local clock.

- The transition shall happen only after bit lock is achieved by all Re-timer Channels that are in  $CL0s$  state.
- The transition may or may not take place on Symbol boundary.
- Each Re-timer Channel in  $CL0s$  state shall transition to Forwarding state. From this point on, a Re-timer Channel shall forward the bit stream it receives from the Lane and stop generating  $CL\_WAKE1.X$  Symbols.
- During the transition from local clock to receiver clock, the Re-timer shall meet the  $SSC\_SLEW\_RATE$  requirement as specified in the USB4 Specification.

After the Re-timer Channels transitioned to Forwarding state, the Channel's receiver will receive SLOS Ordered Sets. The Re-timer shall lock on Symbol Boundary of the SLOS Ordered Set within  $t_{SymbolLockRT}$  time.

#### **4.2.4.3.1.2 CL1/CL2 Exit**

There are three phases that a Re-timer Channel can through when exiting the CL1 or CL2 state on a Gen 2 or Gen 3 Link:

- Phase 1 – Re-timer Channel is transmitting local copies of the  $CL\_WAKE1$  Symbol using its local clock.
- Phase 2 – Re-timer Channel toggles between transmitting local copies of the  $CL\_WAKE1$  Symbol and the copies of the received  $CL\_WAKE2$  Symbol. The Re-timer transmits Symbols using its local clock.
- Phase 3 – Re-timer Channel is transmitting received data using the recovered clock.

A Re-timer Channel will always go through Phases 1 and Phases 3 when exiting the CL1 or CL2 state. A Re-timer Channel may or may not go through Phase 2.

### **Phase 1:**

When a Re-timer detects an LFPS burst of 2 cycles on one of its Lane Adapters, it shall do the following:

1. Send LFPS as follows:
  - The Lane Adapter that detected the LFPS shall send LFPS for at least 5 LFPS cycles and no more than  $t_{LFPSDuration}$ . A Cable Re-timer that was in CL1 shall transmit the first LFPS cycle  $t_{CL1ForwardLFPS}$  time after the first cycle of LFPS on the receiver. A Cable Re-timer that was in CL2 shall transmit the first LFPS cycle  $t_{CL2ForwardLFPS}$  time after the first cycle of LFPS on the receiver.
  - The Corresponding Adapter shall send LFPS until it detects LFPS.
2. Enable the receivers for the Lane Adapter and its Corresponding Adapter.
  - The Re-timer shall wait at least  $t_{CLxIdleRx}$  after a Lane Adapter stops detecting LFPS before enabling the receiver for that Lane Adapter.
3. For each Adapter, after the last LFPS is transmitted, transition the transmitter to Electrical Idle for  $t_{PreData}$ . Then, start transmitting  $CL\_WAKE1.X$  Symbols, where X is the index of the Re-timer provided by the Router that is the target of the  $CL\_WAKE1.X$  Symbols. The Re-timer shall transmit the Symbols using a locally generated, non-SSC, clock.

### **Phase 2:**

When a Re-timer receives 3  $CL\_WAKE2.(X+1)$  Symbols (where X is the Re-timer Index programmed by the Router that is the source of the  $CL\_WAKE2.(X+1)$  Symbols), and if the Re-timer is still transmitting on its local clock in this Re-timer Channel, then the Re-timer shall transition this Re-timer Channel to toggle between transmitting two locally-generated  $CL\_WAKE1.X$  Symbols and transmitting the last two  $CL\_WAKE2.Y$  Symbols received by the Re-timer Channel.  $CL\_WAKE1$  Symbols received by the Port shall not be transmitted while the Port is in toggling mode. Only  $CL\_WAKE2$  Symbols received by the Port are transmitted.

The transition may or may not take place on Symbol boundary.

### **Phase 3:**

After a Re-timer receives 3 back-to-back  $CL\_WAKE2.X$  Symbols (where X is the Re-timer Index programmed by the Router that is the source of the  $CL\_WAKE2.X$  Symbols) on Lane 0 of a Re-timer Channel in a given direction, the Re-timer shall transition all Re-timer Channels in the opposite direction to transmit on the clock recovered from the received traffic rather than on its local clock. A Re-timer Channel shall ignore any received  $CL\_WAKE1.Y$  (where Y is any value) Symbols interleaved with  $CL\_WAKE2.X$  Symbols when it determines the reception of back-to-back  $CL\_WAKE2.X$  Symbols.

- The transition shall happen only after bit lock is achieved by both active receivers in the Re-timer Channel performing the transition.



- The transition may or may not take place on Symbol boundary.
- Each Re-timer Channel performing the transition shall transition to Forwarding state. From this point on, the Re-timer Channel shall forward the bit stream it receives from the Lane and stop generating CL\_WAKE1.X Symbols.
- During the transition from local clock to receiver clock, the Re-timer Channel shall meet the frequency variation requirements as specified in Section 3.1.3.1.1 of the USB4 Specification.

#### **4.2.4.3.1.3 Timing Requirements**

A Re-timer shall meet the following timing requirements during exit from CL0, CL1, or CL2 states:

- A receiver shall complete Symbol lock within tCLxLock of receiving SLOS or CL\_WAKE1.X Symbols.
- A transmitter shall complete the transition to a recovered clock within tSwitchNoSSC if the received clock is a non-SSC clock.
- A transmitter shall complete the transition to a recovered clock within tSwitchSSC if the received clock is an SSC clock.
- A receiver shall complete Symbol Realignment within tSymbolLockRT after Ordered Sets changes.

#### **4.2.4.3.2 Gen 4 Exit from State**

##### **4.2.4.3.2.1 CL0s Exit**

This section describes Re-timer behavior during CL0s exit for a Gen 4 Link.

When a Re-timer detects an LFPS burst on the Lane 0 receiver of a Port with a receiver in Low Power state, the Re-timer shall:

1. Send LFPS on the corresponding transmitter that is in CL0s as follows:
  - In a Cable Re-timer, the first LFPS cycle shall be transmitted tCL1ForwardLFPS time after the first cycle of LFPS on the receiver. It is recommended that an on board re-timer will forward the LFPS within tOBCL1ForwardLFPS timer after the first cycle of LFPS.
  - If the Re-timer entered CL1 or CL2 state while receiving LFPS, it shall go to step 1 in the CL1/CL2 exit flow described in Section 4.2.4.3.2.2.
  - The transmitter shall stop sending LFPS after sending at least 16 LFPS cycles and after the Lane 0 receiver detected CL0s\_EXIT Ordered Set with the *CL0s Phase* field set to 00t.
2. Enable the receivers tCLxIdleRx time after receiving the last LFPS on the Lane 0 receiver.
3. On the corresponding Port:
  - The transmitter shall return to Electrical Idle for tPreData after transmitting the last LFPS cycle.

- All enabled transmitters shall transmit back-to-back Gen 4 TS1 using the TxFFE Preset that was used prior to CL0s entry. If the conditions of step 4 are met, the *Indication* field may be set to 2h, otherwise it shall be set to 1h.

*Note: The point that all enabled transmitters start sending Gen 4 TS 1 is measured from the last LFPS cycle and transition to Electrical Idle of the transmitter that sent the LFPS.*

4. When all the enabled receivers are ready for PAM3 and detect a Gen 4 TS1 with the *Indication* field set to 2h, the corresponding transmitters shall transmit back-to-back Gen 4 TS1 with the *Indication* field set to 2h.
5. When one of the active receivers of the corresponding Port detects a CL0s\_EXIT Ordered Set with the *CL0s Phase* field set to 01t, all enabled transmitters in the corresponding Port shall transmit back-to-back Gen 4 TS2. If the conditions of step 6 are met, the *Indication* field may be set to 4h, otherwise it shall be set to 3h.
6. When all the enabled receivers finished electrical equalization and detect a Gen 4 TS2 with the *Indication* field set to 4h, the corresponding transmitters shall transmit back-to-back Gen 4 TS2 with the *Indication* field set to 4h.
7. The channel shall execute Clock Switch Flow as described in Section 4.1.3.2 within tTS3Detect from receiving Gen 4 TS3 with the *Indication* field set to 5h.
8. The Channel State Machine shall transition to the Forwarding state.

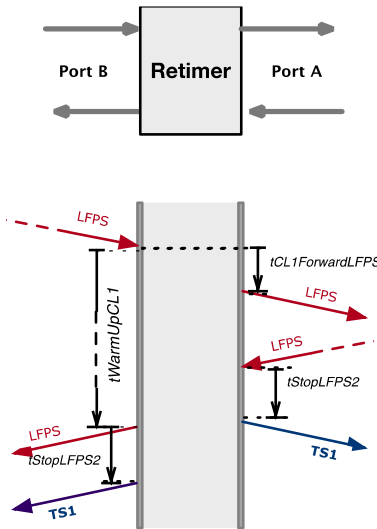
*Note: TxFFE negotiation is not part of CL0s exit flow.*

#### 4.2.4.3.2.2 CL1/CL2 Exit

This section describes Re-timer behavior during CLx exit for a Gen 4 Link. tCLxForwardLFPS refers to using tCL1ForwardLFPS if the Re-timer is in CL1 and tCL2ForwardLFPS if the Re-timer is in CL2. tWarmUpCLx refers to using tWarmUpCL1 if the Re-timer is in CL1 and tWarmUpCL2 if the Re-timer is in CL2. CL1 and CL2 exit sequences are triggered by LFPS reception where the Re-Timer performs on each of its ports LFPS handshake followed by Gen 4 TS1 and Gen 4 TS2 handshakes separately before moving to Clock Switching on both ports. Figure 4-8 illustrates an LFPS handshake for a Cable Re-Timer with Ports A and B and being presented as a reference for demonstrating the sequence rules below. In this example the Re-Timer channels are in CL1 while Port B detects LFPS.

It is recommended for an On-board Re-timer to forward LFPS within tOBCL1ForwardLFPS or tOBCL2ForwardLFPS time for CL1 or CL2 exit accordingly, after receiving the first cycle of LFPS.

Figure 4-8. Retimer CL1 Exit – LFPS Handshake Example



When a Re-timer detects an LFPS burst on the Lane 0 receiver of its port, the Re-timer shall:

1. Transmit LFPS on the corresponding transmitter (e.g. Port A). A Cable Re-timer shall send the first LFPS within  $t_{CLxForwardLFPS}$  time after the first LFPS cycle on the receiver. The transmitters shall stop sending LFPS  $t_{StopLFPS2}$  time after all the following are true:
  - The Re-timer detected LFPS on Lane 0 receiver of the corresponding Port (e.g., Port A).
  - The Re-timer transmitted at least 16 LFPS cycles after detecting LFPS on the corresponding Port's receiver (e.g., Port A).
  - $t_{EnterLFPS3}$  time passed since the Re-timer shut down the corresponding transmitter.
2. Transmit LFPS on the Adapter's transmitter (e.g. Port B). The first LFPS shall be sent within  $t_{WarmUpCLx}$  time after the first LFPS cycle on the receiver. The transmitter shall send at least 16 LFPS cycles. The transmitter shall stop transmitting LFPS  $t_{StopLFPS2}$  after at least one of the following conditions is met:
  - $t_{EnterLFPS3}$  time passed since the Re-timer shut down the Adapter's transmitter (e.g. Port B)
  - The Adapter's receiver (e.g. Port B) is not detecting LFPS
3. On each Port:
  - After the transmitter stops sending LFPS, it shall return to Electrical Idle for  $t_{PreData}$ , then all active transmitters shall start sending back-to-back Gen 4 TS1 using the TxFFE Preset that was used prior to CLx entry.

- After the Lane 0 receiver detects the last LFPS cycle, all enabled receivers shall be enabled for high-speed signal reception. The receivers shall be enabled  $t_{CLxIdleRx}$  time after the end of the last LFPS cycle was received on Lane 0 receiver.
  - When all the enabled receivers are ready for PAM3, all the enabled transmitters shall transmit back-to-back Gen 4 TS1 with the *Indication* field set to 2h. The first Gen 4 TS1 with *indication* field set to 2h shall be sent within  $t_{RxLock}$  from the first received Gen 4 TS1.
  - All enabled transmitters shall transmit back-to-back Gen 4 TS2 with the *Indication* field set to 3h within  $t_{TrainingTransition}$  once all the conditions below are true:
    - i. Each active transmitter sent at least 16 Gen 4 TS1 with the *Indication* field set to 2h.
    - ii. All enabled receivers detect Gen 4 TS1 with the *Indication* field set to 2h or Gen 4 TS2.
  - When all enabled receivers finish PAM3 equalization, all the enabled transmitters shall transmit Gen 4 TS2 with the *Indication* field set to 4h.
4. On each Port, the corresponding transmitters shall execute Clock Switch Flow as described in Section 4.1.3.2 within  $t_{TS3Detect}$  after all the following conditions are true:
- All enabled receivers detect Gen 4 TS3
  - Each active transmitter sent at least 16 Gen 4 TS2 with *Indication* field set to 4h.
  - The corresponding transmitters sent at least 16 Gen 4 TS2 with *indication* field set to 4h
  - All receivers in the corresponding Port detected Gen 4 TS2 with *Indication* field set to 4h or Gen 4 TS3

*Note: TxFFE negotiation is not part of CLx exit flow.*

### 4.3 Lane Decoding

To track entry into CLx states and to participate in exit from CLx states, a Re-timer shall decode Ordered Sets received on its Lane Adapters as defined in the USB4 Specification.



#### IMPLEMENTATION NOTE

*It is recommended that a Re-timer implement RS-FEC error detection. Not implementing RS-FEC error detection may cause the Re-timer to lose track on the RS-FEC activation on the Link and prevent it from entering CLx states.*



#### IMPLEMENTATION NOTE

*The path for decoding Ordered Sets is independent of the forwarding path (see section 4.2.3.2). Decoding Ordered sets does not affect the Ordered Set that is forwarded by the Re-timer.*

4.3.1 Error Cases

Table 4-4 lists the error cases that a Re-timer shall support along with how that error shall be handled.

Table 4-4. Required Error Cases

Error	Event	Response
SLOS detection	Lane Adapter detects 3 SLOS in Forwarding state with RS-FEC on or Lane Adapter detects 15 SLOS in Forwarding state with RS-FEC off.	If RS-FEC decoding is on, turn-off RS-FEC decoding on this Lane in both USB4 Ports and perform Symbol lock on received SLOS.

Table 4-5 lists the additional error cases that a Re-timer may optionally support along with how that error shall be handled.

Table 4-5. Optional Error Cases

Error	Event	Response
RS-FEC Decoder Error	The RS-FEC decoder identifies an uncorrectable error.	Turn off RS-FEC decoding on this Lane. Perform Symbol lock on received SLOS.

4.4 Asymmetric Link

An Asymmetric Link is a Link where a Re-timer has 3 transmitter and 1 receiver in one Port and 3 receivers and 1 transmitter in the other Port. If a Cable Re-timer supports Gen 4, it shall support Asymmetric Link. An Onboard Re-timer may support Asymmetric Link, and it shall communicate this information to the Router in its Router assembly as part of Phase 1 of Lane Initialization. A Re-timer that supports Asymmetric Link shall execute the transition from Symmetric to Asymmetric Link and vice-versa as described in Section 4.4.1.

Router A and Router B give each Re-timer a unique Index. Each Re-timer is required to detect Gen 4 CL\_OFF Ordered Sets with a specific *Index* field as part of the Asymmetric Transition flow. For the Gen 4 CL\_OFF Ordered Set sent by Router A to affect the Re-timer, the *Index* field in it should match the Index given to the Re-timer by Router B.

4.4.1 Asymmetric Link Transitions

This section describes the transition from a Symmetric Link to an Asymmetric Link and vice versa. Example of transitions can be found in the USB4 Specification.

When a Re-timer detects a UNBOND Ordered Set on its receiver, it shall do the following:

1. After detecting a Gen 4 CL\_OFF Ordered Set with the *Index* field that matches the index given to the Re-timer by the Router to which it forward the Gen 4 CL\_OFF Ordered Set, the Re-timer shall shut down the corresponding transmitter tRtTxOff time after the first trit of the first Gen 4 CL\_OFF

Ordered Set was transmitted by the corresponding transmitter. Common Mode voltages shall be maintained.

2. Shut down the receiver that detected the Gen 4 CL\_OFF Ordered Set within tRxShut time after detecting the Gen 4 CL\_OFF Ordered Set. Rx Termination shall be maintained.
3. When the Port receives an LT\_SwitchRx2Tx transaction it shall:
  - a. Wait for tActivateNewTx time.
  - b. Enable an additional transmitter in the Port instead of the receiver that detected the Gen 4 CL\_OFF Ordered Set and set Common Mode voltage on the new transmitter.
  - c. Enable an additional receiver in the corresponding Port, instead of the transmitter that forwarded the Gen 4 CL\_OFF Ordered Set. RX termination shall be set on the new receiver.
  - d. The Re-timer shall change the mapping of the *Gen 4 TxFFE* Register to match the new Link properties.
4. The Re-timer shall forward the LT\_SwitchRx2Tx transaction to its corresponding Port within tForwardSwitch time after receiving the LT\_SwitchRx2Tx transaction.
5. When the Port receives an LT\_SwitchAck transaction it shall forward the transaction to its corresponding Port within tForwardSwitch.
6. The Re-timer shall enable LFPS detection on the new receiver and LFPS transmission on the new transmitter.
7. The Re-timer shall transmit LFPS on the new transmitter when all the below conditions are true:
  - a. The new receiver detects LFPS.
  - b. tActivateNewTx time has elapsed since LT\_SwitchAck was sent.

In a Cable Re-timer, it is recommended that the first LFPS be sent within tCL2ForwardLFPS after detecting the LFPS.

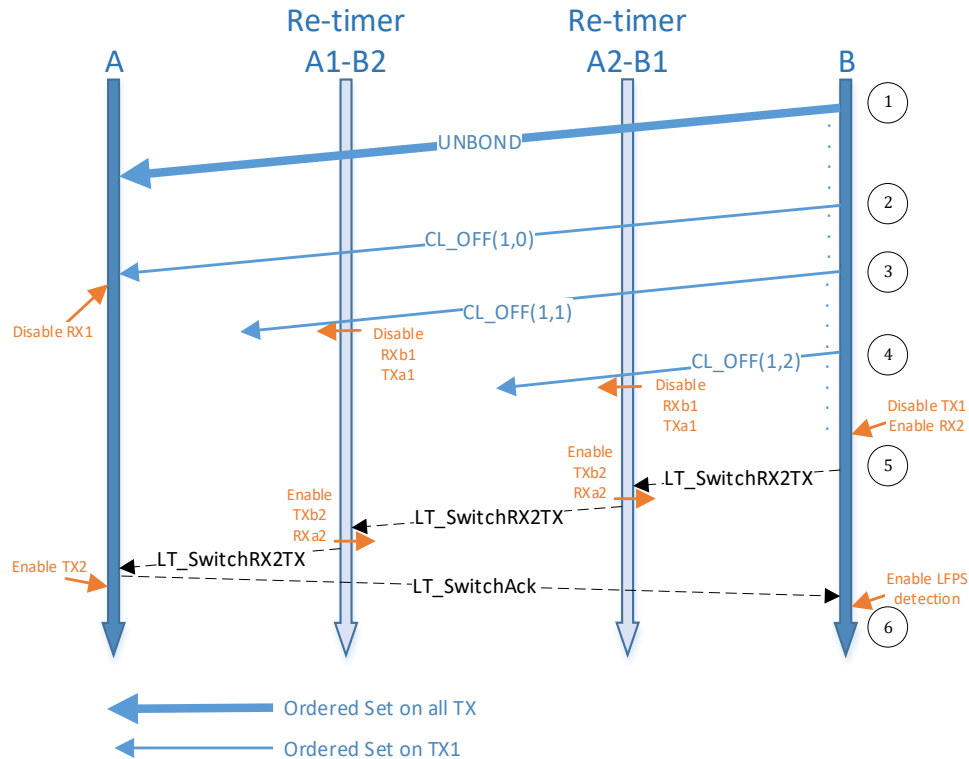
8. When the receivers in the corresponding Port detect a Gen 4 CL0s\_EXIT Ordered Set with the *CL0s Phase* field set to 00t, the new transmitter shall stop transmitting LFPS within tStopLFPS1, transition to Electrical Idle for tPreData, and send Gen 4 TS1 with the *Indication* field set to 1h using the same recovered clock as the existing transmitter(s).
9. The new transmitter and receiver shall execute Gen 4 TxFFE negotiation as described in the USB4 Specification.
10. When the new receiver is ready for PAM3 signaling and detects Gen 4 TS1 with the *Indication* field set to 2h, the new transmitter shall send Gen 4 TS1 with the *Indication* field set to 2h.

11. When the receivers in the corresponding Port detect a Gen 4 CL0s\_EXIT Ordered Set with the *CL0s Phase* field set to 01t, the new transmitter shall transmit Gen 4 TS2 with the *Indication* field set to 3h using the same recovered clock as the existing transmitter(s).
12. When the new receiver finishes Gen 4 TxFFE negotiation and detects Gen 4 TS2 with the *Indication* field set to 4h, the new transmitter shall send Gen 4 TS2 with the *Indication* field set to 4h.
13. When the new receiver detects a Gen 4 TS3 with the *Indication* field set to 5h, the new transmitter shall transmit the recovered data from the new receiver using the same recovered clock as the existing transmitter(s).

*Note: Since the existing transmitter(s) already use a recovered clock, the new transmitters use it when sending Gen 4 TS1 and Gen 4 TS2, unlike regular Lane Initialization or the Low Power state exit flows.*

Figure 4-8 shows an example of a first part of a transition from Symmetric Link to Asymmetric Link where Router B will have 1 transmitter and 3 receivers and Router A will have 3 transmitters and 1 receiver.

**Figure 4-8. Example of Asymmetric Transition**



Re-timer A1-B2 received Index 1 from Router A and Index 2 from Router B. Re-timer A2-B1 received Index 2 from Router A and Index 1 from Router B.

1. Router B sends UNBOND Ordered Sets. After that, Transport Layer data is sent only on transmitter 0.
2. Transmitter 1 sends Gen 4 CL\_OFF with CL state field set to 1 and Index field set to 0 to shut down Router A.
3. Transmitter 1 sends Gen 4 CL\_OFF with CL state field set to 1 and Index field set to 1 to shut down receiver 1 facing Router B and transmitter 1 facing Router A on Re-timer A1-B2. The Index in the Gen 4 CL\_OFF Ordered Set matches the Index given to the Re-timer by Router A.

4. Transmitter 1 sends Gen 4 CL\_OFF with CL state field set to 1 and Index field set to 2 to shut down receiver 1 facing Router B and transmitter 1 facing Router A on Re-timer A2-B1. The Index in the Gen 4 CL\_OFF Ordered Set match the Index given to the Re-timer by Router A. When finished sending the Gen 4 CL\_OFF Ordered Sets, Router B disables transmitter 1 and enables receiver 2 which uses the same physical lines.
5. Router B sends LT\_SwitchRx2Tx transaction. When a Re-timer receives this transaction, it enables transmitter 2 facing Router B and receiver 2 facing Router A. After that the Re-timer forwards the transaction.
6. LFPS detection is enabled in Router B and Re-timers after detecting LT\_SwitchAck transaction.

#### 4.5 Gen 4 Link Recovery

Gen 4 Link Recovery is an autonomous process initiated by Routers in cases where they encounter various uncorrectable error events, see Section 4.4.7 in USB4 Specification. Gen 4 Link Recovery is not applicable for Gen 2 and Gen 3 Links.

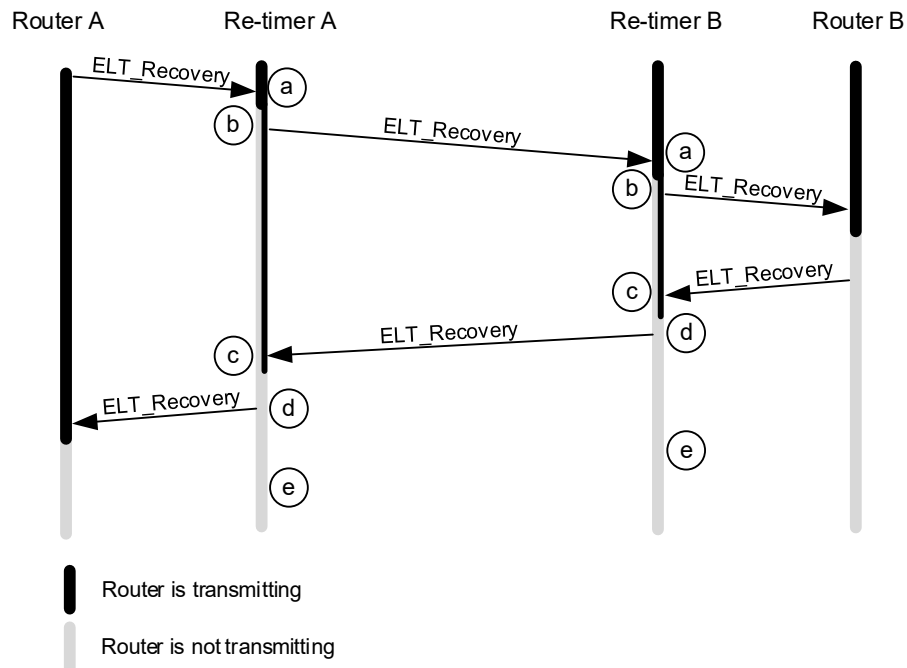
A Re-timer shall support Gen 4 Link Recovery on each USB4 Port that operates with a Gen 4 Link.

When a Re-timer receives an ELT\_Recovery transaction on one of its Ports it shall do the following:

1. Shut down the receiving Port's transmitters within tRecoveryTxOff.
2. Shut down the Corresponding Port's receivers tRecoveryRxOff after shutting down the receiving Port's transmitters.
3. Forward the ELT\_Recovery transaction to the corresponding Port.
4. Transition to Phase 4 in Lane Initialization as described in section 4.1.2.

Figure 4-9 is an example of Gen 4 Link Recovery flow on a Link with 2 Re-timers.

**Figure 4-9. Example of Gen 4 Link Recovery flow on a Link with 2 Re-timers**





- a. The Re-timer receives ELT\_Recovery transaction and shuts down its transmitters facing Router A and corresponding receivers Facing Router B.
- b. After the Re-timer shuts down its transmitters on the Port that received the ELT\_Recovery and their corresponding receivers, it forwards the ELT\_Recovery to its corresponding Port.
- c. The Re-timer receives ELT\_Recovery transaction and shuts down its transmitters facing Router B corresponding receivers Facing Router A.
- d. After the Re-timer shuts down its transmitters on the Port that received the ELT\_Recovery and their corresponding receivers, it forwards the ELT\_Recovery to its corresponding Port.
- e. After forwarding the second ELT\_Recovery, the Re-timer transitions to Phase 4.

#### 4.6 Timing Parameters

Table 4-6 lists the timing parameters for a Re-timer.



#### IMPLEMENTATION NOTE

*When both a Min and a Max value are listed in the table below, an implementation can choose to implement that parameter with any value in the given range. Furthermore, an implementation cannot assume that its Link Partner will use the Max value and must be prepared for Link Partners that use any value between Min and Max (inclusive).*

**Table 4-6. Re-timer Timing Parameters**

Parameter	Description	Min	Max	Units
tSkew	Additional skew allowed for a transmitter between Lane 0 and Lane 1. Also, the difference in propagation delay between Re-timer Channels in a pair of Corresponding Adapters.	--	8	ns
tConnectRx	The time that SBRX will stay at logical high to signal a connect event.	25	--	μs
tDisconnectRx	The time that SBRX will stay at logical low to signal a disconnect event.	14	1000	μs
tLatency2	At Gen 2 speed, the time from when a bit is received to the time it is transmitted by the Corresponding Transmitter.	--	50	ns
tLatency3	At Gen 3 speed, the time from when a bit is received to the time it is transmitted by the Corresponding Transmitter.	--	30	ns
tLatency4	At Gen 4 speed, the time from when a bit is received to the time it is transmitted by the Corresponding Transmitter.	--	30	ns
tPollTxFFE	The rate of polling during the TxFFE flows.	1	5	ms
tRtTxOff	Time of shutting off the transmitters when entering a CLx state or as part of Gen 4 Asymmetric Link Transitions.	0 (Gen 2/3) 50 (Gen 4)	100 (Gen 2/3) 150 (Gen 4)	ns

tCLxLock	The time to achieve Symbol lock during exit from a CLx state	--	60	μs
tSwitchNoSSC	The time to perform clock switch during exit from a CLx state, with a non-SSC receive clock.	--	10	μs
tSwitchSSC	The time to perform clock switch during exit from a CLx state, with an SSC receive clock.	--	75	μs
tRxShut	Time before receiver may shut down.	2000 (Gen 2/3) 50 (Gen 4)	--	ns
tEnterCLx	The time the transmitter transmits DC balanced signal before Channel enters to CLx.	2450	2700	ns
tLROff	Timeout to detect that the Link enters sleep state.	30	50	Ms
tCL1ForwardLFPS	The time from the first LFPS cycle on the receiver to sending the first LFPS cycle on the corresponding transmitter when exiting CL1 on a Cable Re-timer.	--	1	μs
tCL2ForwardLFPS	The time from the first LFPS cycle on the receiver to sending the first LFPS cycle on the corresponding transmitter when exiting CL2 on a Cable Re-timer.	--	10	μs
tForwardWake	The time from detecting a Wake on USB4 event on one Port to forwarding the Wake on USB4 event on the other Port.	--	20	ms
tForwardSwitch	The time from the last bit of an LT_SwitchRx2Tx or LT_SwitchAck on the USB4 Port to forwarding them to the corresponding Port.		10	ms
tTS3Detect	The time from detecting Gen 4 TS3 in the receiver to transiting Gen 4 TS2.clksw in the corresponding transmitter.		2	us
tPreClkSw	The time the transmitters send Gen 4 TS2.clksw pattern with local clock before switching to recovered clock.	2	3	us
tOBCL1ForwardLFPS	The recommended LFPS forwarding time of an On-board Re-timer when existing CL1 or CL0s.	--	10	us
tOBCL2ForwardLFPS	The recommended LFPS forwarding time of an On-board Re-timer when existing CL2.	--	20	us
tSymbolLockRT <sup>1</sup>	Time to complete Symbol Realignment when receiving SLOS on Lane Initialization and CL0S, CL1 and CL2 exit flows		400 (Gen 2) 200 (Gen 3)	ns
<p>Notes:</p> <ol style="list-style-type: none"> <li>On board Re-timer may use higher values of tSymbolLockRT if the Router in the assembly provides sufficient time for the Re-timer to Lock. Given tLatency2/3 of the On-board Re-timer and tTraining Transition and tSymbolLock of the Router of the assembly, the tSymbolLockRT of the Re-timer should be:  <math display="block">T_{SymbolLockRT} &lt; 2 * t_{Latency2/3} + t_{SymbolLock} + t_{TrainingTransition} + 10ns + 90ns * (4 - Gen)</math> </li> </ol>				

*Note:  $tWarmUpCL1$ ,  $tWarmUpCL2$ ,  $tCmdResponse$ ,  $tStopLFPS1$ ,  $tStopLFPS2$ ,  $tLFPSDuration$ ,  $tEnterLFPS1$ ,  $tEnterLFPS2$ ,  $tCLxIdleRx$ , and  $tActivateNewTx$  are defined in the USB4 Specification.*

## 5 Port Operations

When the Opcode register in SB Register Space is written, a Re-timer Port shall execute the Port Operation associated with the Opcode register using the information in the Metadata and Data registers.

After executing the Port Operation, the Re-timer Port updates the Opcode, Metadata, and Data register as follows:

- If the Re-timer Port successfully completed the Port Operation, it shall set the Opcode register to 0. The Re-timer Port shall update the Metadata register with completion metadata (if the Port Operation is defined to return metadata), and the Data register with completion data (if the Port Operation is defined to return data).
- Else, if the Port Operation is not supported, the Re-timer Port shall set the Opcode register to a FourCC value of “!CMD” (444D4321h). The USB4 Port may update the Metadata and Data registers. However, any updates will be ignored by the Connection Manager.
- Else, the Re-timer Port shall set the Opcode register to a FourCC value of “ERR ” (20525245h) to indicate that the Port Operation is supported, but could not be completed. The USB4 Port may update the Metadata and Data registers. However, any updates will be ignored by the Connection Manager.

A Re-timer Port shall send an ELT\_OpDone Transaction after it completes a Port Operation (see Section 4.1.1.2.2 in the USB4 Specification).

A Re-timer Port shall support the Port Operations listed in Table 5-1 with the following exceptions:

- A Re-timer that does not support an NVM is not required to support NVM\_SET\_OFFSET, NVM\_BLOCK\_WRITE, NVM\_AUTH\_WRITE and NVM\_READ Port Operations.
- A Re-timer that supports Gen 4 shall support SQ128 patterns and/or SQ224 pattern in the SET\_TX\_COMPLIANCE Port Operation
- A Re-timer that supports Gen 4 may optionally support the FEC\_ERRORS\_STAT Port Operation.

**Table 5-1. Port Operation Supported by a Re-timer (Required)**

Port Operation	Opcode <sup>5</sup>	Operation		Completion		Reference
		Metadata DW	Data DWs	Metadata DW	Data DWs	
QUERY_LAST_RE-TIMER	LAST (5453414Ch)	0	0	1	0	Section 5.1.1
QUERY_CABLE_RE-TIMER	CBLR (524C4243h)	0	0	1	0	Section 5.1.2

<sup>5</sup> Byte 0 of the Opcode is the rightmost byte of the hexadecimal representation.

SET_TX_COMPLIANCE	TXCM (4D435854h)	1	0	0	0	USB4 Specification
SET_RX_COMPLIANCE	RXCM (4D435852h)	1	0	0	0	USB4 Specification
ENTER_EI_TEST	EEIT (54494545h)	1	0	0	0	USB4 Specification
LFPS_TEST	LFPT (5450464Ch)	1	0	0	0	USB4 Specification
START_BER_TEST	SBER (52454253h)	1	0	0	0	USB4 Specification
END_BER_TEST	EBER (52454245h)	1	0	0	2	USB4 Specification
END_BURST_TEST	BBER (52454242h)	1	0	0	3	USB4 Specification
READ_BURST_TEST	RBER (52454252h)	1	0	0	3	USB4 Specification
SET_INBOUND_SBTX	LSUP (5055534Ch)	0	0	0	0	Section 5.2.1
UNSET_INBOUND_SBTX	USUP (50555355h)	0	0	0	0	Section 5.2.2
GET_NVM_SECTOR_SIZE	GNSS (53534E47h)	0	0	1	0	Section 5.2.3
NVM_SET_OFFSET	BOPS (53504F42h)	1	0	0	0	Section 5.2.4
NVM_BLOCK_WRITE	BLKW (574B4C42h)	0	16	0	0	Section 5.2.5
NVM_AUTH_WRITE	AUTH (48545541h)	0	0	1	0	Section 5.2.6
NVM_READ	AFRR (52524641h)	1	0	0	0 to 16	Section 5.2.7
READ_LANE_MARGIN_CAP	RDCP (50434452h)	0	0	0	2	USB4 Specification
RUN_HW_LANE_MARGINING	RHMG (474D4852h)	1	0	0	2	USB4 Specification
RUN_SW_LANE_MARGINING	RSMG (474D5352h)	1	0	0	0	USB4 Specification
READ_SW_MARGIN_ERR	RDSW (57534452h)	0	0	1	0	USB4 Specification
SET_CLX_LATENCY_TOL	SCLT	1	0	0	0	USB4 Specification

QUERY_CLX_LATENCY_TOL	QCLT	0	0	1	0	USB4 Specification
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## 5.1 Enumerating Port Operations

The Port Operations defined in the subsections below are used to identify and enumerate the Re-timers in a Link. The following is an example Port Operation sequence used for the purpose:

1. Set the *Index* field to 1 to access a Re-timer with a Re-timer Index that equals 1.
2. Issue an Addresses RT Command that reads register 0 in the SB Register Space of the Re-timer.
3. Poll the *Pending* bit in the USB4 Port Capability.
4. Read the result of the Command from the *No Response* bit in the USB4 Port Capability.
5. If the *No Response* bit is set to 0b, repeat from step 2, incrementing the *Index* field value. If the *No Response* bit is set to 1b, the number of Re-timers is the last *Index* field value sent minus 1. If no Re-timer is detected, exit. Else, go to next step.
6. Set the *Index* field to 1 to access a Re-timer with a Re-timer Index that equals 1.
7. Issue a QUERY\_CABLE\_RE-TIMER Operation to the Re-timer. Issue consecutive QUERY\_CABLE\_RE-TIMER Operations, each time incrementing the *Index* field, as long as the response contains a *Cable Re-timer* bit set to 1b and as long as the last Re-timer has not been queried. Capture the number of Cable Re-timers identified. If all Re-timers have been identified, exit. Else, continue to the next step.
8. Issue a QUERY\_LAST\_RE-TIMER Operation to the Re-timer with the *Index* field value. Issue consecutive QUERY\_LAST\_RE-TIMER Operations, each time incrementing the *Index* field, as long as the response contains a *Last* bit set to 0b and as long as the last Re-timer has not been queried. Capture the number of On-Board Re-timers identified. If all Re-timers have been identified, exit. Else, continue to the next step.
  - If Cable Re-timers have been identified in step 7, then the Re-timers identified in step 8 are far-end Re-timers.
  - If Cable Re-timers have not been identified in step 7, and the last Re-timer accessed in step 8 returned a *Last* bit set equal to 0b, then the Re-timers identified in step 8 are far-end Re-timers.
  - Else, the Re-timers identified in step 8 are near-end On-Board Re-timers.

Increment the *Index* field. Issue a QUERY\_CABLE\_RE-TIMER Operation to the Re-timer. Issue consecutive QUERY\_CABLE\_RE-TIMER Operations, each time incrementing the *Index* field, as long as the response contains a *Cable Re-timer* bit set to 1b and as long as the last Re-timer has not been queried. Capture the number of Cable Re-timers identified. If all Re-timers have been identified, exit. Else, continue to the next step.

Any Re-timer with a Re-timer Index equal or larger than the *Index* field value is a far-end On-Board Re-timer.

### 5.1.1 QUERY\_LAST\_RE-TIMER

The QUERY\_LAST\_RE-TIMER Port Operation checks if an On-Board Re-timer is directly connected to a USB Type-C connector.

This Port Operation does not have Operation Metadata.

This Port Operation does not have Operation Data.

The Completion for this Operation does not have Completion Data.

Table 5-2 describes the Completion Metadata that a Re-timer shall return.

**Table 5-2. QUERY\_LAST\_RE-TIMER Completion Metadata**

DW	Bits	Field Name and Description
0	0	<b>Last</b>  0b – The target of the Operation is not an On-Board Re-timer directly connected to a USB Type-C connector.  1b – The target of the Operation is an On-Board Re-timer directly connected to a USB Type-C connector.
0	31:1	<b>Reserved</b>

### 5.1.2 QUERY\_CABLE\_RE-TIMER

The QUERY\_CABLE\_RE-TIMER Port Operation checks if a Re-timer is a Cable Re-timer.

This Port Operation does not have Operation Metadata.

This Port Operation does not have Operation Data.

The Completion for this Operation does not have Completion Data.

Table 5-3 describes the Completion Metadata that a Re-timer shall return.

**Table 5-3. QUERY\_CABLE\_RE-TIMER Completion Metadata**

DW	Bits	Field Name and Description
0	0	<b>Cable Re-timer</b>  0b – The target of the Operation is not a Cable Re-timer  1b – The target of the Operation is a Cable Re-timer
0	31:1	<b>Reserved</b>

## 5.2 NVM Port Operations

The Port Operations defined in the subsections below are used to update the NVM of a Re-timer through the Sideband Channel. This section applies to On-Board Re-timers and Cable Re-timers.

The following is an example of a Port Operation sequence used by software to enable Sideband Channel Transactions with On-Board Re-timers before updating the NVM of an On-Board Re-timer:

1. Software issues a ROUTER\_OFFLINE\_MODE Port Operation to a Router with the *Enter Offline Mode* bit set to 0b. After receiving such a Port Operation, the Router ignores connect and disconnect events until it receives a ROUTER\_OFFLINE\_MODE Port Operation with the *Enter Offline Mode* bit set to 1b (see step 2 in sequence below to exit this mode).
2. Software issues an ENUMERATE\_RE-TIMERS Port Operation, which causes the Router to send an RT Broadcast Transaction.
3. Software issues a SET\_INBOUND\_SBTX Port Operation to each On-Board Re-timer, starting with the Re-timer with Re-timer Index =1. The Port Operation enables Sideband Channel Transactions on the SBTX line from the Re-timer towards the Router.

The following is an example of a Port Operation sequence used by software to update the NVM of a Re-timer:

1. Software issues a GET\_NVM\_SECTOR\_SIZE Operation to read the sector size of the NVM.
2. Software issues a NVM\_SET\_OFFSET Port Operation, which sets the first location in NVM to be written by the following NVM\_BLOCK\_WRITE Port Operation.
3. Software issues a sequence of NVM\_BLOCK\_WRITE Port Operation, each writing a 64B block of data to NVM.
  - Following a NVM\_BLOCK\_WRITE Port Operation, if the value of the *Opcode* register is “ERR”, software repeats all previous NVM\_BLOCK\_WRITE Port Operation. The first Port Operation to be issued is a NVM\_SET\_OFFSET Port Operation that sets the location in NVM of the first block to be rewritten.
4. Software issues a NVM\_AUTH\_WRITE Port Operation to indicate to the target that all data was sent to the target. After receiving the NVM\_AUTH\_WRITE Port Operation, the target performs an authentication check over the data written.

The following Port Operation sequence is used by software to validate the results of the NVM update:

1. Software then waits for at least 5 seconds from the completion of the NVM\_AUTH\_WRITE Port Operation. It then issues another ENUMERATE\_RE-TIMERS Port Operation, which causes the Router to send an RT Broadcast Transaction.
2. Software reads the results of the NVM\_AUTH\_WRITE Port Operation. If the *Status* field in the Completion Metadata is 0h, the update completed successfully. Otherwise, software repeats all previous NVM\_BLOCK\_WRITE Port Operation. The first Port Operation to be issued is a NVM\_SET\_OFFSET Port Operation that sets the location in NVM of the first block to be rewritten, followed by issuing one or more NVM\_BLOCK\_WRITE Port Operation again.



If this is the case of updating the NVM of an On-Board Re-timer, then the following Port Operation sequence is used by software to exit this mode:

1. Software issues a UNSET\_INBOUND\_SBTX Port Operation to each On-Board Re-timer, starting with the Re-timer closest to the USB Type-C connector. The Port Operation sets the SBTX line from the Re-timer towards the Router to the logical level of the SBRX line from the direction of the USB Type-C connector.
2. Software issues an ROUTER\_OFFLINE\_MODE Port Operation to the Router with the *Enter Offline Mode* bit set to 1b. After receiving such a Port Operation, the Router is ready to process connect events.

### **5.2.1 SET\_INBOUND\_SBTX**

Software uses the SET\_INBOUND\_SBTX Port Operation to enable Sideband Channel Transactions on the SBTX of a Re-timer. The SBTX that faces towards the Router is enabled.

A Re-timer that is the target of the Port Operation drives its SBTX line in the direction of the Router to logical high and enables the transmission of RT Responses towards the Router. The Re-timer that is the target of the Port Operation is not required to send an RT Response for the first SET\_INBOUND\_SBTX Port Operation.

*Note: This Port Operation does not cause bi-directional communication on SBTX. Communication over SBTX remains unidirectional.*

This Port Operation does not have Operation Metadata.

This Port Operation does not have Operation Data.

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

### **5.2.2 UNSET\_INBOUND\_SBTX**

A Re-timer that is the target of the UNSET\_INBOUND\_SBTX Port Operation drives its SBTX line in the direction of the Router to the logical level of the SBRX line from the direction of the USB Type-C connector.

This Port Operation does not have Operation Metadata.

This Port Operation does not have Operation Data.

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

### **5.2.3 GET\_NVM\_SECTOR\_SIZE**

The GET\_NVM\_SECTOR\_SIZE Port Operation returns the size of an NVM sector.

This Port Operation does not have Operation Metadata.

This Port Operation does not have Operation Data.

The Completion for this Operation does not have Completion Data.

Table 5-4 describes the Completion Metadata that a Re-timer shall return.

**Table 5-4. GET\_NVM\_SECTOR\_SIZE Completion Metadata**

DW	Bits	Field Name and Description
0	23:0	<b>Sector Size</b> Equal to the sector size of the NVM in bytes. For example, a value of 1000h indicates a sector size of 4KB.
0	31:24	<b>Reserved</b>

#### 5.2.4 NVM\_SET\_OFFSET

The NVM\_SET\_OFFSET Port Operation sets the first location in NVM to be written by the following NVM\_BLOCK\_WRITE Port Operation.

This Port Operation does not have Operation Data. Table 5-5 describes the Operation Metadata for this Port Operation.

**Table 5-5. NVM\_SET\_OFFSET Operation Metadata**

DW	Bits	Field Name and Description
0	1:0	<b>Reserved</b>
0	23:2	<b>NVM Offset</b> This field contains the first address to be written relative to the base address of the region been written. NVM Offset is incremented by 16 after each NVM_BLOCK_WRITE (see Section NVM_BLOCK_WRITE). Address is specified in DWs.
0	31:24	<b>Reserved</b>

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

### 5.2.5 NVM\_BLOCK\_WRITE

The NVM\_BLOCK\_WRITE Port Operation writes 64B NVM, starting at the address equal to the NVM Offset. A Re-timer shall increment its NVM Offset value by 16 after executing this Port Operation (even if the write operation fails).

If the write operation fails, the Port Operation shall complete with an “ERR ” status.

This Port Operation does not have Operation Metadata. Table 5-6 describes the Operation Data for this Port Operation.

**Table 5-6. NVM\_BLOCK\_WRITE Operation Data**

DW	Bits	Field Name and Description
0	31:0	<b>DW0</b> The first Doubleword, to be written into NVM at NVM Offset address.
1	31:0	<b>DW1</b> The second Doubleword, to be written into NVM at the next NVM Offset.
...	31:0	...
15	31:0	<b>DW15</b> The last Doubleword of this Port Operation, to be written into NVM at the next NVM Offset.

The Completion for this Operation does not have Completion Metadata.

The Completion for this Operation does not have Completion Data.

### 5.2.6 NVM\_AUTH\_WRITE

The NVM\_AUTH\_WRITE Port Operation indicates to the Re-timer that all data was sent to it. The Re-timer performs an authentication check over the data written. The authentication check is implementation specific and outside the scope of this specification.

Following the execution of an NVM\_AUTH\_WRITE Port Operation, the Re-timer shall maintain the SBTX line of its Router-Facing USB4 Port with the same state as before the execution of the Operation. The Re-timer may maintain its Re-timer Index value but is not required to do so.

This Port Operation does not have Operation Metadata.

This Port Operation does not have Operation Data.

The Completion for this Operation does not have Completion Data.

Table 5-7 describes the Completion Metadata that a Re-timer shall return.

**Table 5-7. NVM\_AUTH\_WRITE Completion Metadata**

DW	Bits	Field Name and Description
0	5:0	<b>Status</b> 0h - Authentication completed successfully 1h - Authentication Failed 2h - Retry NVM write Else - Reserved
0	31:6	<b>Reserved</b>

If the *Status* field in the Completion Metadata is 2h, then software repeats all previous NVM\_BLOCK\_WRITE Port Operation. The first Port Operation to be issued is a NVM\_SET\_OFFSET Port Operation that sets the location in NVM of the first block to be rewritten, followed by issuing a NVM\_AUTH\_WRITE Port Operation again.

### 5.2.7 NVM\_READ

The NVM\_READ Port Operation reads up to 64 bytes from NVM.

This Port Operation does not have Operation Data. Table 5-8 describes the Operation Metadata.

**Table 5-8. NVM\_READ Operation Metadata**

DW	Bits	Field Name and Description
0	1:0	<b>Reserved</b>
0	23:2	<b>NVM Offset</b> This field contains the first address to be read relative to the base address of the region being read. NVM Offset is specified in DWs.
0	27:24	<b>Length</b> Number of Doublewords that shall be read starting from the <i>NVM Offset</i> field value. If this field is zero, then 16 DWs are read.
0	31:28	<b>Reserved</b>

The Completion for this Operation does not have Completion Metadata.

If completed successfully, the Port Operation shall return *Length* number of Doublewords of Completion Data as described in Table 5-9.

Table 5-9. NVM\_READ Completion Data

DW	Bits	Field Name and Description
0	31:0	<b>DW0</b> The first Doubleword read from NVM at <i>NVM Offset</i> address.
1	31:0	<b>DW1</b> The second Doubleword read from NVM at the next NVM Offset.
...	31:0	...
15	31:0	<b>DW15</b> The last Doubleword read from NVM at the next NVM Offset.

5.3 Receiver Lane Margining Port Operations

A USB4 Port shall perform the Receiver Lane Margining Port Operations as defined in the USB4 Specification. A Re-timer shall execute a Receiver Lane Margining Port Operation on the Port on which the operation is received.

## 6 Interoperability with Thunderbolt™ 3 (TBT3) Systems

This section defines the requirements for an On-Board Re-timer to operate as part of a Link that includes a Thunderbolt 3 cable and/or one or more Thunderbolt 3 Routers. It also defines the requirements for a Cable Re-timer to operate as part of a Link that includes a Thunderbolt 3 Router.

A Cable Re-timer shall support the requirements defined in this chapter.

An On-Board Re-timer may optionally support the requirements defined in this chapter.

### 6.1 Electrical Layer

A Cable Re-timer shall support TBT3-Compatible Gen 2 speed (10.3125 Gbps) and TBT3-Compatible Gen 3 speed (20.625 Gbps).

An On-Board Re-timer shall support TBT3-Compatible Gen 2 speed (10.3125 Gbps).

### 6.2 Logical Layer

#### 6.2.1 Sideband Channel

When operating in a TBT3-Compatible Link, a Re-timer uses either a TBT3-Compatible Sideband Channel or a USB4-Compatible Sideband Channel, depending on what the Routers on each side of the Link support (see Section 13.2.1 in the USB4 Specification for more detail). An On-board Re-timer shall operate with a USB4-Compatible Sideband Channel when it receives a Broadcast Transaction with the USB4-Compatible Sideband Channel bit set to 1b. Otherwise, it shall operate with a TBT3-Compatible Sideband Channel.

*Note: The link speed and type of Sideband channel that an On-Board Re-timer operates with is determined only by the USB4/TBT3 Transactions it receives and is independent of the information obtained over USB PD in Phase 1 of Link Initialization.*

This section defines the additional Sideband Channel behavior that a Re-timer shall implement when operating in a TBT3-Compatible that uses a TBT3-Compatible Sideband Channel.

*Note: A TBT3-Compatible Link with a TBT3-Compatible Sideband does not support CLx states and is therefore not required to decode symbols on the Lanes.*

##### 6.2.1.1 Bidirectional Re-timers

A bidirectional Re-timer is a Re-timer that sends Transactions on its SBRX wire. A unidirectional Re-timer does not send Transaction on its SBRX wire. The Cable Re-timers in a Thunderbolt active cable are bidirectional. The Router and On-Board Re-timers in a Thunderbolt host or device are unidirectional.

This section defines when a USB4 Re-timer does and does not behave as a bidirectional Re-timer in order to maintain TBT3-Compatability.

##### 6.2.1.1.1 Cable Re-Timers

A Cable Re-timer shall implement a unidirectional behavior when the Sideband Channel operates in TBT3-Compatible mode. A Cable Re-timer does not need to implement bi-directional behavior.

#### **6.2.1.1.2 On-Board Re-Timers**

An On-Board Re-timer that is adjacent to a USB Type-C connector shall implement both unidirectional and bidirectional behavior.

- When the Re-timer is adjacent to a Thunderbolt Cable Re-timer, it shall operate with a bidirectional Sideband Channel on its Cable-Facing USB4 Port. The Router-Facing USB4 Port shall operate with a unidirectional Sideband Channel.
- When the Re-timer is not adjacent to a Thunderbolt Cable Re-timer, it shall operate with a unidirectional Sideband Channel on both USB4 Ports.

An On-Board Re-timer that is not adjacent to a USB Type-C connector shall implement unidirectional behavior on both USB4 Ports.

When a USB4 Port on an On-Board Re-timer is operating in bidirectional mode:

- The USB4 Port shall support concurrent reception of Transactions on SBTX and on SBRX.
- The USB4 Port shall drive its SBTX for up to 2-bit times after the last Stop bit of an AT Command.
- The USB4 Port shall not forward a received Transaction if it is still waiting for a Response to a n AT Command it sent.

#### **6.2.1.2 Transactions**

##### **6.2.1.2.1 LT Transactions**

A Cable Re-timer shall send an LT\_Resume Transaction to its Router Facing Port after the *TX Active* bit is set to 1b in the Lane 0 Adapter in its Router Facing Port.

The behavior of a Cable Re-timer towards its Cable Facing Port is implementation specific.

If an On-board Re-timer is adjacent to a USB Type-C connector and it receives an LT\_Resume Transaction on its Router Facing Port, it shall forward the LT\_Resume Transaction to its Cable Facing Port only after the *Forward Switch Done* bit is set to 1b in the Lane 0 Adapter in its Cable Facing Port. Otherwise, an On-board Re-timer shall forward an LT\_Resume Transaction received on one USB4 Port to its other USB4 Port.

*Note: The requirements above make sure that a Re-timer adjacent to a USB Type-C connector, whether it is a Cable Re-timer or an On-board Re-timer, sends the LT\_Resume transaction towards the USB Type-C connector only after the transmitter facing the USB Type-C connector is sending data received by its corresponding receiver using a recovered clock with SSC.*

A Cable Re-timer shall forward an LT\_Resume2 Transaction received on its Router-Facing USB4 Port to its Cable-Facing USB4 Port.

*Note: The LT\_Resume2 Transaction is forwarded by the Cable Re-timer to indicate it is transmitting data received by its corresponding receiver using a recovered clock with SSC. This indication can be used by the other Cable Re-timer for the internal TxFFE negotiation.*

A Re-timer shall forward a received LT\_Gen\_2 Transaction to its other USB4 Port.

A Re-timer shall forward a received LT\_Gen\_3 Transaction to its other USB4 Port.

#### 6.2.1.2.2 AT Transactions

##### 6.2.1.2.2.1 Cable Re-timers

A Cable Re-timer shall support the Bounce mechanism as defined in the USB4 Specification.

A Cable Re-timer shall not initiate AT Commands.

A Cable Re-timer shall respond to a received AT Command that has the *Recipient* bit set to 0b and the *Bounce* bit set to 0b. Else, it shall forward the received AT Command to its other USB4 Port.

##### 6.2.1.2.2.2 On-Board Re-timers

An On-Board Re-timer may generate AT Commands (see Section 6.2.1.3.3).

An On-Board Re-timer shall respond to a received AT Command with the *Recipient* bit set to 1b that access the TxFFE Register in the SB Register Space. It shall forward other received AT Commands to its other USB4 Port.

When an On-Board Re-timer receives an AT Response with the *Recipient* bit set to 1b that accesses the TxFFE Register in SB Register Space, it shall process that AT Response and shall not forward the AT Response to its other USB4 Port. It shall forward all other received AT Responses to its other USB4 Port.

#### 6.2.1.2.3 RT Transactions

An On-Board Re-timer that is adjacent to a USB Type-C connector shall not forward Broadcast RT Transactions towards the cable.

It is recommended that an On-Board Re-timer not forward Addressed RT Transactions towards the cable.

#### 6.2.1.2.4 SB Register Space

The SB Register Space of a Re-timer shall have the additional fields described in Table 6-1 and Table 6-2.

**Table 6-1. Re-timer SB Registers**

Register	Size (Bytes)	Name	Description
13	8	TxFFE	Used to set the TxFFE parameters of transmitters. Bytes 4-7 in this register are Rsvd for On-Board Re-timers.



Table 6-2. SB Register Fields

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
13	TxFFE	2	5	<b>Forward Switch Done (Lane 0)</b> Indicates that the transmitter transmits using the Router's clock: 0b – Transmitter uses a Re-timer's clock 1b – Transmitter uses Router's clock	RO	0b
		3	5	<b>Forward Switch Done (Lane 1)</b> Indicates that the transmitter transmits using the Router's clock: 0b – Transmitter uses a Re-timer's clock 1b – Transmitter uses Router's clock	RO	0b
		4 <sup>6</sup>	3:0	<b>TxFFE Request (Lane 0)</b> Identifies one of 16 predefined TxFFE configurations requested by the receiver.	RW	0
			4	<b>Rsvd</b>	Rsvd	0b
			5	<b>Rx Active (Lane 0)</b> Indicates whether or not the receiver is active: 0b – Receiver is inactive 1b – Receiver is active	RW	0b
			6	<b>Rsvd</b>	Rsvd	0
			7	<b>New Request (Lane 0)</b> Indicates whether or not the receiver is providing a new index in the <i>TxFFE Request</i> field: 0b – Receiver is still processing a previous TxFFE configuration 1b – Receiver is providing a new index in the <i>TxFFE Request</i> field	RW	0b
		5 <sup>7</sup>	3:0	<b>TxFFE Request (Lane 1)</b> Identifies one of 16 predefined TxFFE configurations requested by the receiver.	RW	0
			4	<b>Rsvd</b>	Rsvd	0b

<sup>6</sup> This byte is the *Partner Rx Status & TxFFE Request* byte for Lane 0

<sup>7</sup> This byte is the *Partner Rx Status & TxFFE Request* byte for Lane 1

Register	Register Name	Byte	Bits	Field Name and Description	Type	Default Value
			5	<b>Rx Active (Lane 1)</b> Indicates whether or not the receiver is active: 0b – Receiver is inactive 1b – Receiver is active	RW	0b
			6	<b>Rsvd</b>	Rsvd	0
			7	<b>New Request (Lane 1)</b> Indicates whether or not the receiver is providing a new index in the <i>TxFEE Request</i> field: 0b – Receiver is still processing a previous TxFEE configuration 1b – Receiver is providing a new index in the <i>TxFEE Request</i> field	RW	0b
		6 <sup>8</sup>	3:0	<b>TxFEE setting (Lane 0)</b> Index of the TxFEE configuration loaded the transmitter.	RW	0
			6:4	<b>Rsvd</b>	Rsvd	0
			7	<b>Tx Active (Lane 0)</b> Indicates whether or not the transmitter is transmitting a valid signal: 0b – Transmitter is not transmitting a valid signal 1b – Transmitter is transmitting a valid signal	RW	0b
		7 <sup>9</sup>	3:0	<b>TxFEE setting (Lane 1)</b> Index of the TxFEE configuration loaded the transmitter.	RW	0
			6:4	<b>Rsvd</b>	Rsvd	0
			7	<b>Tx Active (Lane 1)</b> Indicates whether or not the transmitter is transmitting a valid signal: 0b – Transmitter is not transmitting a valid signal 1b – Transmitter is transmitting a valid signal	RW	0b

<sup>8</sup> This byte is the Partner Tx Status byte for Lane 0

<sup>9</sup> This byte is the Partner Tx Status byte for Lane 1

### 6.2.1.3 Lane Initialization

#### 6.2.1.3.1 Phase 1 – Determination of Initial Conditions

During phase 1, an On-Board Re-timer uses the mechanism defined in the USB Type-C Specification and the USB PD Specification to obtain the following additional information for each of its USB4 Ports:

- Cable incorporates Thunderbolt 3 bidirectional Re-timers (True/False)
- Passive or Active Cable (Passive/Active)

A Re-timer shall not proceed to phase 2 unless Thunderbolt 3 Mode is established on the Link.

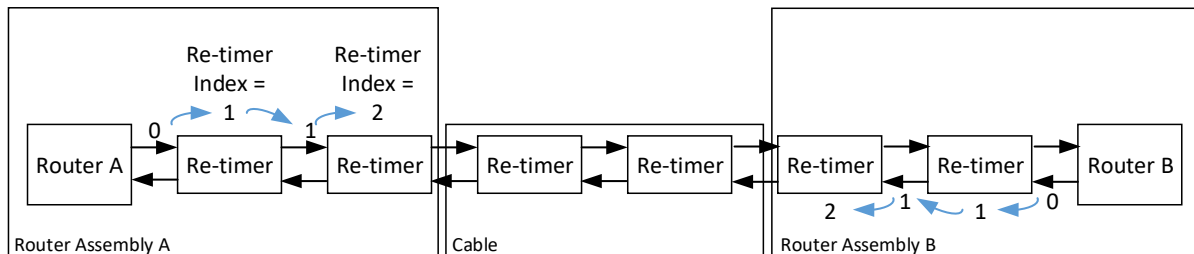
#### 6.2.1.3.2 Phase 4 – Lane Parameters Synchronization

This section replaces Section 4.1.2.4.

An On-Board Re-timer shall decode Broadcast RT Transactions, LT\_Gen\_2 Transactions, and LT\_Gen\_3 Transactions, and shall use the Link parameter from the most recently received Transaction.

Figure 6-1 depicts an example of how a Broadcast RT Transaction is used to assign indexes in a Thunderbolt 3-compatible system to a Link with 6 Re-timers. Each Router enumerates the On-Board Re-timers in its Router Assembly.

**Figure 6-1. Propagation of Broadcast RT Transactions**



A Cable Re-timer shall decode LT\_Gen\_2 Transactions and LT\_Gen\_3 Transactions, and shall use the Link parameter from the most recently received LT Transaction.

If, on any USB4 Port, a Cable Re-timer detects LT\_Resume for Lane 0 before it detects at least one LT\_Gen\_2 Transaction or LT\_Gen\_3 Transaction for Lane 1, then the Re-timer shall keep the Lane 1 Adapters in both USB4 Ports in the CLd state and shall not proceed with Lane Initialization.

When a Re-timer detects LT\_Resume on any Lane of any USB4 Port, it shall transition to phase 5.

#### 6.2.1.3.3 Phase 5 – Lane Equalization

This section replaces Section 4.1.2.5.

Re-timer type and Lane Adapter position determine which TxFFE negotiation flow a transmitter or receiver performs. Table 6-3 lists which TxFFE negotiation flows a transmitter or receiver shall perform in phase 5.

**Table 6-3. TxFFE Negotiation flows**

Re-timer Type	Lane Adapter Position	Rx/Tx	TxFFE Negotiation Flow	Reference	Transactions
On-Board Re-timer	Adjacent to a Router or an On-Board Re-timer in the same Router Assembly	Receiver or Transmitter	Symmetric TxFFE Negotiation flow	USB4 Specification	Addressed RT Transactions with the <i>Index</i> field set to 0
On Board Re-timer	Adjacent to a Cable Re-timer	Transmitter only	Asymmetric TxFFE Parameter Negotiation with a Transmitting Primary Partner flow	USB4 Specification	AT Transactions: requests are sent with the <i>Recipient</i> bit set to 0, process responses with <i>Recipient</i> bit set to 1
On-Board Re-timer	Adjacent to a Cable Re-timer	Receiver only	Asymmetric TxFFE Parameter Negotiation with a Receiving Primary Partner	USB4 Specification	AT Transactions: send transactions with the <i>Recipient</i> bit set to 0, process responses with <i>Recipient</i> bit set to 1
On-Board Re-timer	Adjacent to a Passive Cable	Receiver or Transmitter	Symmetric TxFFE Negotiation flow	USB4 Specification	AT Transactions: send requests and process responses with the <i>Recipient</i> bit set to 1
Cable Re-timer	Adjacent to a USB Type-C connector	Receiver only	Asymmetric TxFFE Parameter Negotiation with a Receiving Subordinate Partner	Section 6.2.1.3.3.1	AT Transactions: process requests with the <i>Recipient</i> bit set to 0, send responses with <i>Recipient</i> bit set to 1
Cable Re-timer	Adjacent to a USB Type-C connector	Transmitter only	Asymmetric TxFFE Parameter Negotiation with a Transmitting Subordinate Partner	Section 6.2.1.3.3.2	AT Transactions: process requests with the <i>Recipient</i> bit set to 0, send responses with <i>Recipient</i> bit set to 1

The following rules determine the behavior of an On-Board Re-timer in phase 5:

- An On-Board Re-timer Lane Adapter that is not adjacent to a USB Type-C connector shall turn on its transmitter when the *Rx Active* bit of its Corresponding Receiver is set to 1b. It shall start transmitting CL\_WAKE1.X Symbols, where X is the Re-timer Index assigned by the Router that is the target of the CL\_WAKE1.X Symbols. The transmitter shall use a locally generated, non-SSC clock to transmit the CL\_WAKE1.X Symbols. It shall then set the *Tx Active* bit for the Lane Adapter to 1b.

- A Re-timer adjacent to a USB Type-C connector shall set the *Clock Switch Done* bit to 1b in a Router-Facing Adapter when all receivers in Router-Facing Adapters complete TxFFE negotiation. The Re-timer may turn on transmitters adjacent to the USB Type-C connector. Once the *Clock Switch Done* bit is set to 1b, a transmitter adjacent to a USB Type-C connector that is turned on shall forward the bit stream it receives from the Corresponding Receiver using a recovered clock.
- When all of the following are true, a transmitter that is not adjacent to a USB Type-C connector shall stop using the local clock, shall start using the recovered clock from the Corresponding Receiver, and shall forward the bit stream it receives from the Corresponding Receiver:
  - In the transmitter's USB4 Port, TxFFE negotiation is complete between all transmitters and their Adjacent Receivers.
  - In the USB4 Port opposite the transmitter's USB4 Port, TxFFE negotiation is complete between all receivers and their Adjacent Transmitter.
  - The *Clock Switch Done* bit for Lane 0 of the transmitter's adjacent USB4 Port is 1b.
- A Re-timer adjacent to a Router shall set the *Forward Switch Done* bit to 1b in a Lane Adapter of a Cable-Facing USB4 Port when transmitter of the Lane Adapter is using the receiver clock from the Corresponding Receiver.
- A Re-timer shall set the *Forward Switch Done* bit to 1b in a Lane Adapter if the *Forward Switch Done* bit is set to 1b in the adjacent USB4 Port of the Corresponding Receiver.
- When the *Forward Switch Done* bit is set to 1b in an adapter adjacent to a USB Type-C connector, the Lane Adapter shall turn on its transmitter, if it has not done so already. It shall then set the *Tx Active* bit to 1b and perform TxFFE Parameter Negotiation.
- When an On-Board Re-timer transmitter completes TxFFE negotiation with a Cable Re-timer receiver, the transmitter shall send an LT\_Resume2 Transaction. The *LSELane* field in the LT\_Resume2 Transaction shall equal the Lane number associated with the transmitter.

The following rules determine the behavior of a Cable Re-timer in phase 5.

- A Cable Re-timer shall set the *Tx Active* bit to 1b in a Router-Facing Adapter when the Lane Adapter is transmitting the bit stream received by a Lane Adapter at the other end of the Cable, and transmission uses the recovered clock from the Lane Adapter at the other end of the Cable.
- The flow between two Cable Re-timers is implementation specific.

#### 6.2.1.3.3.1 Asymmetric TxFFE Parameter Negotiation with a Receiving Subordinate Partner

During TxFFE negotiation, the transmitter negotiates TxFFE parameters with the receiver at the other end. The transmitting end is defined as the Primary Partner. The receiving end is defined as the Subordinate Partner. The Primary Partner sends AT Command to the Subordinate Partner and the Subordinate Partner sends AT Responses to the Primary Partner.

#### Receiver flow:

The steps that the receiver shall perform to complete negotiation are listed below:

1. The receiver shall set the following initial values on entry to Phase 5:
  - Local Rx Status & TxFFE Request byte of the TxFFE register
    - *Rx Locked* bit = 0b
    - *TxFFE Request* field = index of an initial set of TXFFE parameters
    - *Rx Active* bit = 0b
    - *New Request* bit = 0b
  - *Partner Tx Status* byte of the TxFFE register
    - *Tx Active* bit = 0b
    - Request Done bit = 0b
2. The receiver shall evaluate the value of the *Tx Active* bit in the *Partner Tx Status* byte of the *TxFFE* register:
  - If *Tx Active* = 1b (i.e. the transmitter is transmitting), then the receiver shall enable the receiver, set *Rx Active* bit to 1b, and continue to Step 3.
  - Else, repeat Step 2 within tPollTxFFE.
3. The receiver shall evaluate its behavior. If equalization is complete, the receiver shall set the *Rx Locked* field in the *Local Rx Status & TxFFE Request* byte to 1b.
4. The receiver shall do the following:
  - If the *Rx Locked* bit is set to 1b, negotiation is complete and no further TxFFE negotiation steps shall be taken.
  - Else:
    - *TxFFE Request* field shall be set to the index of a selected set of TXFFE parameters.
    - *New Request* bit shall be set to 1b to indicate the receiver is providing a new TxFFE index.
5. Continue to Step 6 only after sending a read Response with the updated values of its TxFFE Register.
6. On reception of an AT Command with a write Command targeting its *Partner Tx Status* byte of the *TxFFE* register, the receiver shall:
  - If (*Tx Active* = 1b) AND (*TxFFE setting* = value of *TxFFE Request* in the *Local Rx Status & TxFFE Request* byte), go to Step 7.

- Else, repeat Step 6.
7. The receiver shall evaluate its receiver behavior. If equalization is complete, the receiver shall set the *Rx Locked* field in the *Local Rx Status & TxFFE Request* byte to 1b.
  8. The receiver shall set the *New Request* field in the *Local Rx Status & TxFFE Request* byte to 0b.
  9. On reception of an AT command with a read Command targeting the TxFFE register go to Step 4.

#### 6.2.1.3.3.2 Asymmetric TxFFE Parameter Negotiation with a Transmitting Subordinate Partner

During TxFFE negotiation, the transmitter negotiates TxFFE parameters with the receiver at the other end. The receiving end is defined as the Primary Partner. The transmitting end is defined as the Subordinate Partner. The Primary Partner sends AT Command to the Subordinate Partner and the Subordinate Partner sends AT Responses to the Primary Partner.

#### Transmitter flow:

The steps that the transmitter shall perform to complete negotiation are listed below:

1. The transmitter shall set the following initial values on entry to Phase 5:
  - *Local Tx Status* byte of the TxFFE register
    - *Tx Active* bit = 1b
    - *Request Done* bit = 0b
    - *TxFFE Setting* field = index of an initial set of TxFFE parameters
  - *Partner Rx Status & TxFFE Request* byte of the TxFFE register
    - *New Request* bit = 0b
2. On reception of an AT Command with a write Command targeting the *Partner Rx Status & TxFFE Request* byte of the TxFFE register, the transmitter shall:
  - If (*New Request* = 0b), repeat Step 2.
  - Else, continue to Step 3.
3. Load one of 16 predefined TxFFE configurations that matches the *TxFFE Request* field of the received AT Command.
4. Send an AT Response to indicate the transmitter is using the new TxFFE request.
5. On reception of an AT Command with a write Command targeting the *Partner Rx Status & TxFFE Request* byte of the TxFFE register, the transmitter shall:

- If (*New Request* = 1b), repeat Step 4.
- Else, continue to Step 2.

*Note: Step 2 is the final step of this flow, the transmitter won't get an indication about the receiver lock status and will wait for the next request even when TxFFE negotiation is done.*

## 6.2.2 Re-timer Channel Layer State Machine

### 6.2.2.1 CLd State

#### 6.2.2.1.1 Behavior in State

In addition to the conditions described in Section 4.2.1.2, a Re-timer Channel shall begin Lane Initialization in phase 4 when:

- If the Re-timer Channel entered this state after detecting an LT\_Fall Transaction, then:
  - The Re-timer Channel for Lane 0 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction with the *Lane0 Enabled* bit set to 1b, an LT\_Gen\_2 Transaction with the *LSELane* bit set to 0b, or an LT\_Gen\_3 Transaction with the *LSELane* bit set to 0b.
  - The Re-timer Channel for Lane 1 shall start Lane Initialization when the Re-timer receives a Broadcast RT Transaction with the *Lane1 Enabled* bit set to 1b, an LT\_Gen\_2 Transaction with the *LSELane* bit set to 1b, or an LT\_Gen\_3 Transaction with the *LSELane* bit set to 1b.

#### 6.2.2.2 CLx States

If the Sideband Channel operates in USB4 Mode, a Re-timer shall support low power capabilities as defined in Section 4.2.4. Else, the Re-timer shall not support low power capabilities.



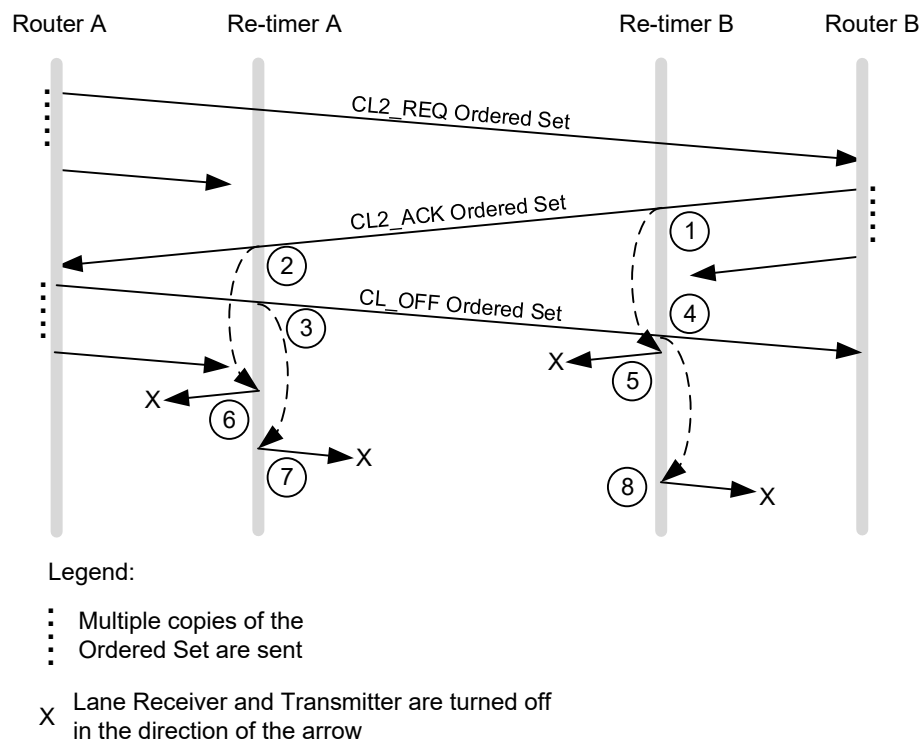
## A. Examples of Entry to Low Power State for Gen 2 and Gen 3

This section contains examples of Lane Adapter behavior during entry to CL2, CL1, or CL0s states for a Gen 2 or Gen 3 Link.

### A.1 Successful Entry to CL2 State

Figure A-1 shows an example of CL2 entry where two Re-timers are in between the Routers with Lane Adapters entering the CL2 state. In the example, Re-timer A is adjacent to Router A and Re-timer B is adjacent to Router B. Router A initiates entry to CL2 state.

**Figure A-1. Successful Entry to CL2 State**



The following steps take place in Figure A-1:

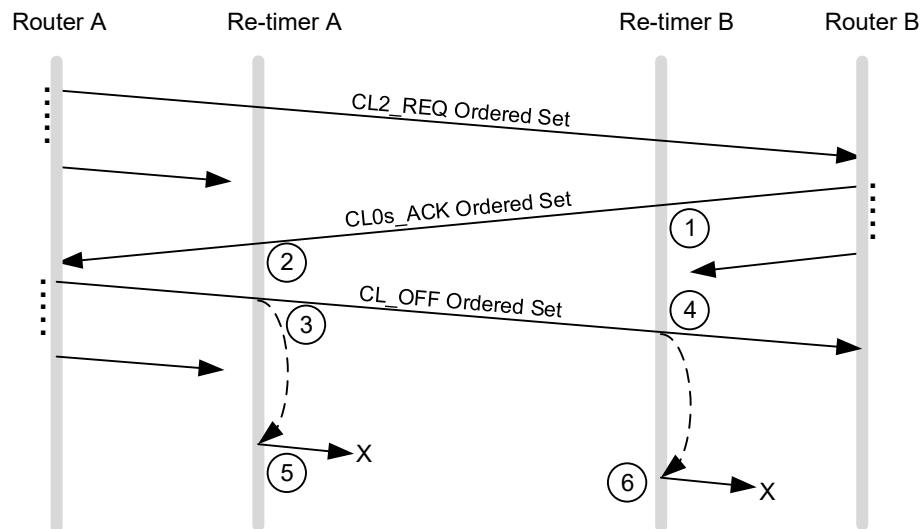
1. Re-timer B detects 3 back-to-back CL2\_ACK Ordered Sets and starts a CL2\_ACK Counter
2. Re-timer A detects 3 back-to-back CL2\_ACK Ordered Sets and starts a CL2\_ACK Counter.
3. Re-timer A detects 3 back-to-back CL\_OFF Ordered Sets and starts a CL\_OFF Counter.
4. Re-timer B detects 3 back-to-back CL\_OFF Ordered Sets and starts a CL\_OFF Counter.

5. Re-timer B's CL2\_ACK Counter reaches a count of 372. Re-timer B then powers down the receiver facing Router B and its Corresponding Transmitter.
6. Re-timer A's CL2\_ACK Counter reaches a count 372. Re-timer A then powers down the transmitter facing Router A and its Corresponding Receiver.
7. Re-timer A's CL\_OFF Counter reaches a count of 372. Re-timer A then powers down the receiver facing Router A and its Corresponding Transmitter.
8. Re-timer B's CL\_OFF Counter reaches a count of 372. Re-timer B then powers down the transmitter facing Router B and its Corresponding Receiver.

## A.2 Successful entry to CL0s State

Figure A-2 shows an example of CL0s entry where two Re-timers are in between the Routers with Lane Adapters entering the CL0s state. In the example, Re-timer A is adjacent to Router A and Re-timer B is adjacent to Router B. Router A initiates entry to CL0s.

**Figure A-2. Successful Entry to CL0s State**



The following steps take place in Figure A-2:

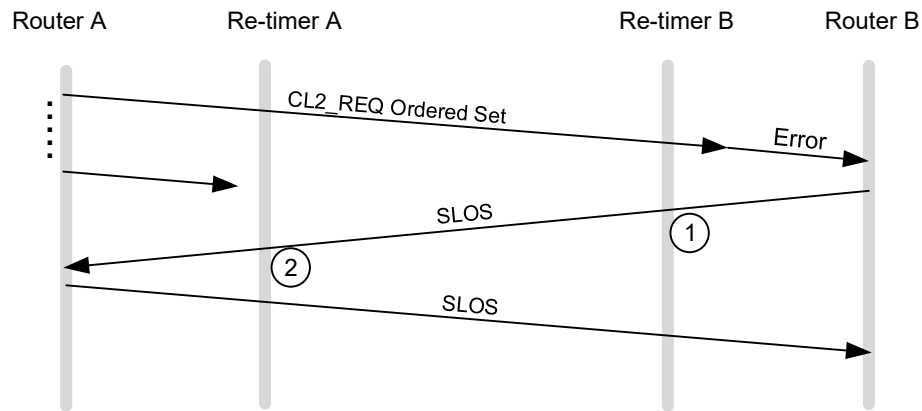
1. Re-timer B detects 3 back-to-back CL0s\_ACK Ordered Sets and starts a CL0s\_ACK Counter.
2. Re-timer A detects 3 back-to-back CL0s\_ACK Ordered Sets and starts a CL0s\_ACK Counter.
3. Re-timer A detects 3 back-to-back CL\_OFF Ordered Sets and starts a CL\_OFF Counter.
4. Re-timer B detects 3 back-to-back CL\_OFF Ordered Sets and starts a CL\_OFF Counter.

5. Re-timer A's CL\_OFF Counter reaches a count of 372. Re-timer A then powers down the receiver facing Router A and its Corresponding Transmitter.
6. Re-timer B's CL\_OFF Counter reaches a count of 372. Re-timer B then powers down the transmitter facing Router B and its Corresponding Receiver.

### A.3 Error in CL2\_REQ Ordered Sets

Figure A-3 shows an example of an attempt by Router A to enter CL2 state, where the CL2\_REQ Ordered Sets are received with errors by Router B. In the example, Re-timer A is adjacent to Router and Re-timer B is adjacent to Router B. Router A initiates entry to CL2.

**Figure A-3. Error in CL2\_REQ Ordered Sets**



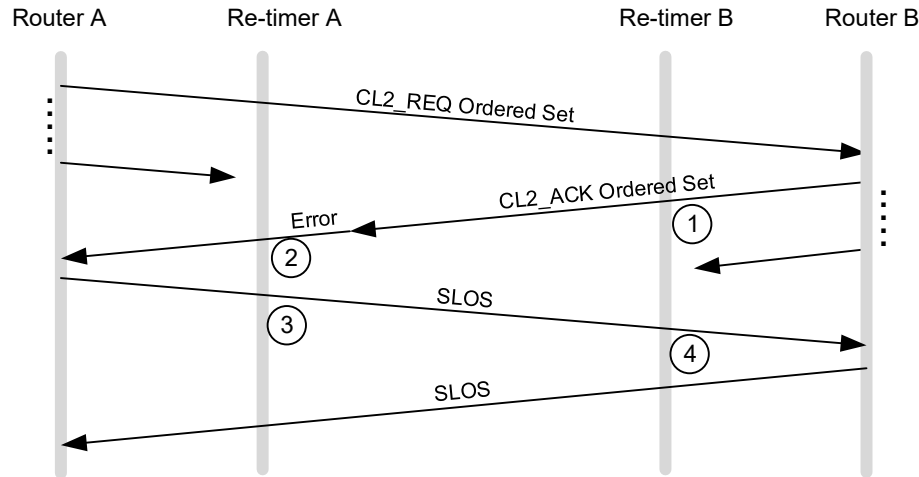
The following steps take place in Figure A-3:

1. Re-timer B detects SLOS or Link errors coming from Router B.
  - If the Re-timer detects errors, it disables RS-FEC in the direction of the errors to allow detection of SLOS.
  - If the Re-timer detects 15 SLOS Symbols, it disables RS-FEC in both directions.
2. Re-timer A detects SLOS or Link errors.
  - If the Re-timer detects errors, it disables RS-FEC in the direction of the errors to allow detection of SLOS.
  - If the Re-timer detects 15 SLOS Symbols, it disables RS-FEC in both directions.
3. Each Re-timer continues with Symbol lock.

#### A.4 Error in CL2\_ACK Ordered Sets

Figure A-4 shows an example of an attempt by Router A to enter CL2 state, where the CL2\_ACK Ordered Sets are received with errors by Router A. In the example, Re-timer A is adjacent to Router A and Re-timer B is adjacent to Router B. Router A initiates entry to CL2.

**Figure A-4. Error in CL2\_ACK Ordered Sets**



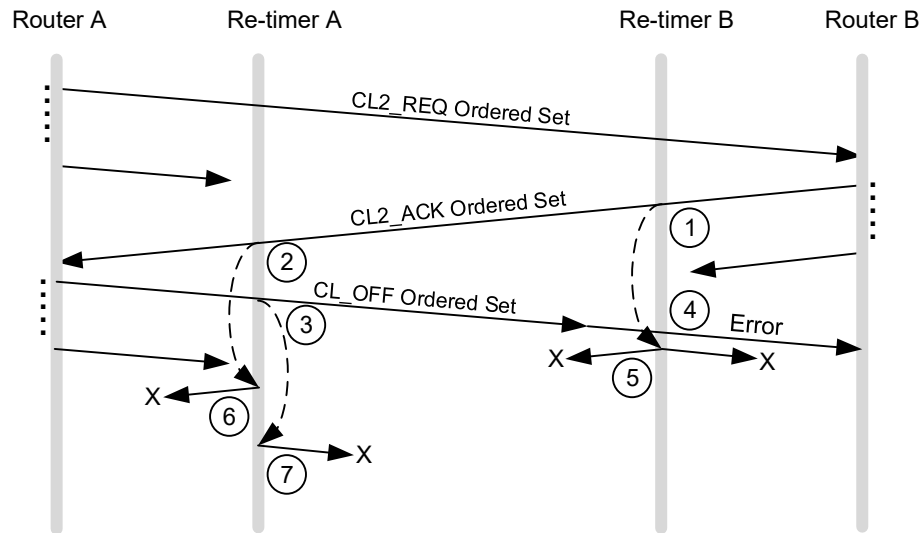
The following steps take place in Figure A-4:

1. Re-timer B detects 3 back-to-back CL2\_ACK Ordered Sets and starts a CL2\_ACK Counter.
  - Re-timer A detects Link errors coming from Router B. It disables RS-FEC in the direction of the errors to allow detection of SLOS.
2. Re-timer A detects 15 SLOS Symbols coming from Router A. It disables RS-FEC in both directions.
3. Re-timer B detects 15 SLOS Symbols. It disables RS-FEC in both directions. It also clears the CL2\_ACK Counter to zero.

#### A.5 Error in CL\_OFF Ordered Sets

Figure A-5 shows an example of an attempt by Router A to enter CL2 state, where the CL\_OFF Ordered Sets are received with errors by Router B. In the example, Re-timer A is adjacent to Router A and Re-timer B is adjacent to Router B. Router A initiates entry to CL2.

Figure A-5. Error in CL\_OFF Ordered Sets



The following steps take place in Figure A-5:

1. Re-timer B detects 3 back-to-back CL2\_ACK Ordered Sets and starts a CL2\_ACK Counter.
2. Re-timer A detects 3 back-to-back CL2\_ACK Ordered Sets and starts a CL2\_ACK Counter.
3. Re-timer A detects 3 back-to-back CL\_OFF Ordered Sets and starts a CL\_OFF Counter.
4. Re-timer B detects Link errors. It disables RS-FEC in the direction of the errors to allow detection of SLOS.
5. Re-timer B's CL2\_ACK Counter reaches a count of 372. Re-timer B then powers down the receivers and the transmitters in both directions.
6. Re-timer A's CL2\_ACK Counter reaches a count of 372. Re-timer A then powers down the transmitter facing Router A and its Corresponding Receiver.
7. Re-timer A's CL\_OFF Counter reaches a count of 372. Re-timer A then powers down the receiver facing Router A and its Corresponding Transmitter.